Network Protocol Acceleration Platform (NPAP)

- TCP/UDP/IP Solutions for FPGAs

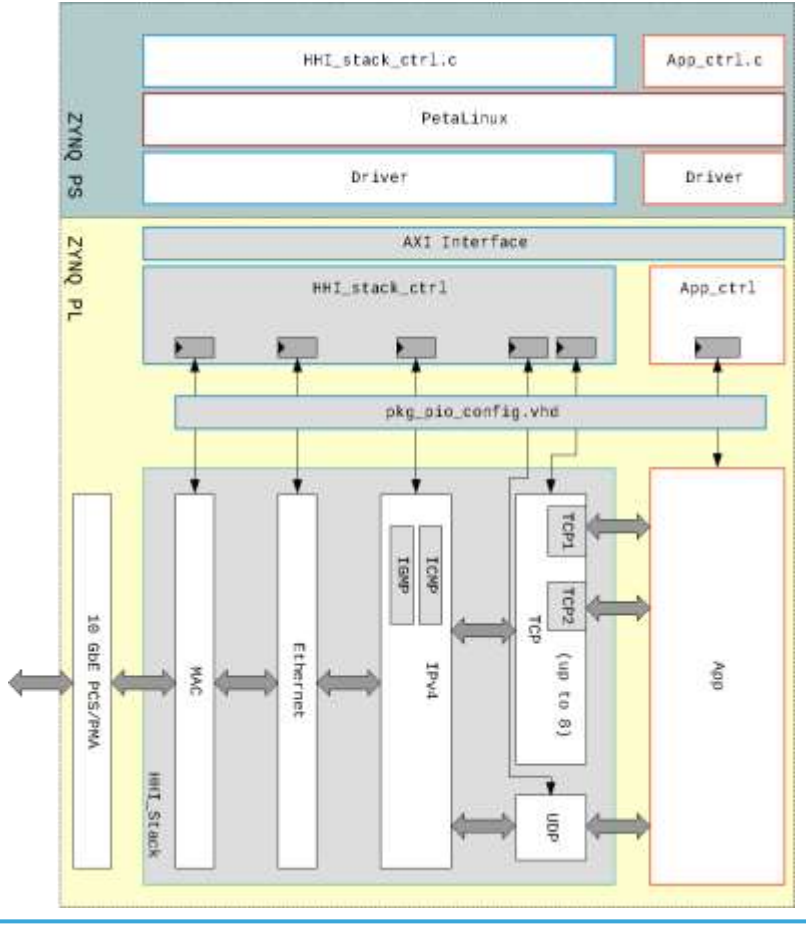
Accelerating and Offloading Network Protocol Processing for multiple 1GigE, 10GigE ports.

Application Use Cases

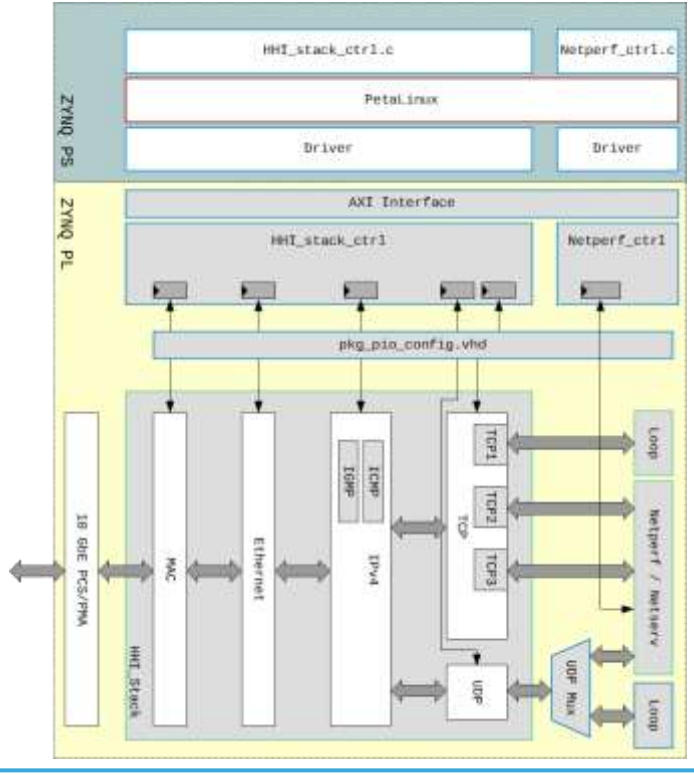
- Bring full TCP/UDP/IP connectivity to FPGAs even when there is no CPU available. Accelerate CPUs by offloading TCP/UDP/IP processing into programmable logic.
- Complete and customizable turn-key solutions and IP cores based on the TCP/UDP/IP stack from the Fraunhofer Heinrich-Hertz-Institute (HHI).
- All processing for MAC / Ethernet / IPv4 / UDP / TCP is implemented in parameterizable HDL code, synthesizable to modern FPGAs.
- User applications can either be implemented in FPGA logic (“Full Acceleration”) or in software via application-specific interfaces to CPUs (“Offloading”).

NPAP Example System

- Highly modular TCP/UDP/IP stack implementation in synthesizable HDL
- Parameterizable for 8-bit (1GigE) or 128-bit (10GigE, 40GigE) data width
- Multiple, parallel TCP engines for scalable processing
- Network Interface Card functionality with Bypass (optional)
- Supports Vivado design flow with High-Level Synthesis design option
- Evaluation on Xilinx Zynq-7000 series All-Programmable SoC



NPAP Evaluation System for Xilinx Zynq-7000



- Targeted to Xilinx Zynq-7045 on ZC706
  - Dual-Core ARM A9MP
  - Xilinx PetaLinux
  - Netperf and TCP-Loopback examples
  - SFP+ for 10GigE via Twinax or Fibre

NPAP Resource Estimates for 10 GigE (128-bit data width)

- Vivado 2014.2 targeting XC7Z045 (Vivado 2014.4 support in works)
  - Full stack with UDP and 2 dedicated TCP engines ~30k LUTs
  - For each additional TCP engine add ~10k LUTs

Instance	Module	Total LUTs	Logic LUTs	LUT RAMs	SRLs	FFs	RAMB36	RAMB18	DSP48 Blocks
wrapper_mac_10gStack	(top)	29459	28425	904	130	25727	50	6	4
(wrapper_mac_10gStack)	(top)	241	241	0	0	0	0	0	0
i_10GStack	Wrapper_LL_IP_TCP__parameterized0	27045	26013	904	128	24644	50	6	4
g0.i_tcpTxMux	TcpTxMux__parameterized0	0	0	0	0	3	0	0	0
gen_WithUdp.i_udp	wrapper_udp__parameterized0	3538	3350	92	96	3732	14	0	0
gen_tcpConnections[0].i_tcp	Wrapper_TCP__parameterized0	9347	8963	384	0	7938	16	3	2
gen_tcpConnections[1].i_tcp	Wrapper_TCP__parameterized0_1	9349	8965	384	0	7938	16	3	2
iBusScheduler8	BusScheduler8__parameterized0	568	568	0	0	31	0	0	0
i_internetLayer	Wrapper_IP__parameterized0	2989	2913	44	32	3437	2	0	0
i_netLayerConv	MacNetworkLayerConversion__parameterized0	139	139	0	0	72	0	0	0
i_networkLayer	Wrapper_Networklayer__parameterized0	1125	1125	0	0	1491	2	0	0
i_txLinkResetSync	ResetSync__parameterized0_2	0	0	0	0	2	0	0	0
i_ResetStretch_aux	ResetStretch__parameterized0	75	74	0	1	35	0	0	0
i_ResetStretch_stack	ResetStretch__parameterized2	75	74	0	1	34	0	0	0
i_clk_stretch	clk_stretch	1	1	0	0	29	0	0	0
i_gen100ms	GenClk100ms__parameterized0	69	69	0	0	30	0	0	0
i_mac10GbE	mac10Gbe_Wrapper__parameterized0	1957	1957	0	0	955	0	0	0
(i_mac10GbE)	mac10Gbe_Wrapper__parameterized0	0	0	0	0	1	0	0	0
i_mac10Gbe	mac10Gbe__parameterized0	1957	1957	0	0	954	0	0	0

NPAP Resource Estimates for 1GigE (8-bit data width)

- Vivado 2014.2 targeting XC7Z045 (Vivado 2014.4 support in works)
  - Full stack with UDP and 2 dedicated TCP engines ~13k LUTs
  - For each additional TCP engine add ~5k LUTs

Instance	Module	Total LUTs	Logic LUTs	LUT RAMs	SRLs SRLs	FFs FFs	RAMB36 RAMB36	RAMB18 RAMB18	DSP48 Blocks
wrapper_mac_10gStack	(top)	13308	12494	812	2	11617	35	5	4
(wrapper_mac_10gStack)	(top)	256	8	248	0	0	0	0	2
i_10GStack	Wrapper_LL_IP_TCP__parameterized0	12780	12216	564	0	11461	35	5	2
(i_10GStack)	Wrapper_LL_IP_TCP__parameterized0	39	39	0	0	1	0	0	0
g0.i_tcpTxMux	TcpTxMux__parameterized0	1	1	0	0	2	0	0	0
gen_WithUdp.i_udp	wrapper_udp__parameterized0	710	618	92	0	1173	13	2	0
gen_tcpConnections[0].i_tcp	Wrapper_TCP__parameterized0	5295	5059	236	0	4380	11	1	1
gen_tcpConnections[1].i_tcp	Wrapper_TCP__parameterized0_0	5295	5059	236	0	4380	11	1	1
iBusScheduler8	BusScheduler8__parameterized0	257	257	0	0	28	0	0	0
i_internetLayer	Wrapper_IP__parameterized0	1154	1154	0	0	1475	0	1	0
i_netLayerConv	MacNetworkLayerConversion__parameterized0	29	29	0	0	20	0	0	0
i_txLinkResetSync	ResetSync__parameterized0_1	0	0	0	0	2	0	0	0
i_ResetStretch_aux	ResetStretch__parameterized0	75	74	0	1	35	0	0	0
i_ResetStretch_stack	ResetStretch__parameterized2	75	74	0	1	34	0	0	0
i_clk_stretch	clk_stretch	1	1	0	0	29	0	0	0
i_gen100ms	GenClk100ms__parameterized0	69	69	0	0	30	0	0	0
i_mac10GbE	mac10Gbe_Wrapper__parameterized0	56	56	0	0	28	0	0	0
i_mac10Gbe	mac10Gbe__parameterized0	56	56	0	0	28	0	0	0

NPAP – Technology from Fraunhofer Heinrich-Hertz-Institute