

Fraunhofer Heinrich-Hertz-Institute partners with MLE to market the proven TCP/IP & UDP Network Protocol Acceleration Platform (NPAP). This customizable solution enables high-bandwidth, low-latency communication solutions for FPGA- and ASIC-based systems for multiple links at 1Gbit/s, 10Gbit/s, and beyond.

## Application Use Cases

- Bring full TCP/UDP/IP connectivity to FPGAs even if no CPU available (“Full Acceleration”). Accelerate CPUs by offloading TCP/UDP/IP processing into programmable logic (“Offloading”).
- Complete and customizable turn-key solutions and IP cores based on the TCP/UDP/IP stack from the Fraunhofer Heinrich-Hertz-Institute (HHI).
- All MAC / Ethernet / IPv4 / UDP / TCP processing is implemented in HDL code, synthesizable to modern FPGAs.
- User applications can either be implemented in FPGA logic or in software via application-specific interfaces to CPUs.

## Key Features

- Highly modular TCP/UDP/IP stack implementation in synthesizable HDL
- Parameterizable for 8-bit (1GigE) or 128-bit (10GigE, 40GigE) data width
- Multiple, parallel TCP engines for scalable processing
- Network Interface Card functionality with Bypass (optional)
- Point-to-point or LAN capable
- Full line rate of  $TPR_{max} = 9.5896$  Gbps
- TCP R/W latency of  $T_{TR(W)} \geq 1.4 \mu s$
- UDP R/W latency of  $T_{UR(W)} \geq 0.75 \mu s$
- Round trip time of  $RTT_{min} \geq 2.25 \mu s$

## Exemplary NIC Implementation



Low profile PCIe x8 Gen2 Board with XC6VHX380T and XC7K410T, QDR2 SRAM, DDR3 DRAM, 1x 40GbE, 4x 10GbE

## License Models and Availability

- IP core for FPGA and ASIC
- complete reference design
- low-profile PCIe NIC w/ FPGA
- customized turn-key solution
- Application-specific R&D services

## Contact MLE

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## Evaluation System for Xilinx Zynq-7000

- Targeted to Xilinx Zynq-7045 on ZC706
- Dual-Core ARM A9MP runs Xilinx PetaLinux
- Netperf and TCP-Loopback examples
- SFP+ for 10GigE via Twinax or Fibre
- Supports Vivado design flow with High-Level Synthesis design option
- Evaluation on Xilinx Zynq-7000 series All-Programmable SoC

### 1 GigE Resource Count (8-bit )

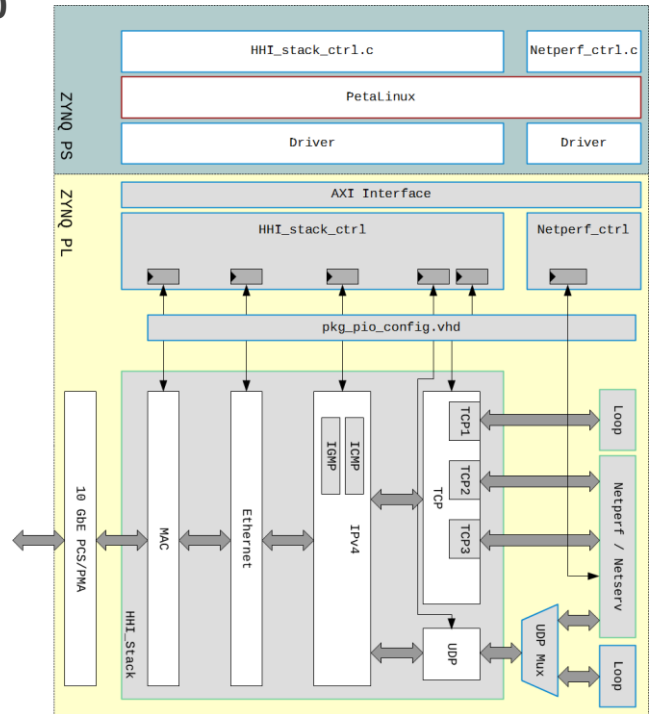
Vivado 2014.4 targeting XC7Z045

- Full stack (UDP and 2 TCP engines) ~13k LUTs
- For each additional TCP engine ~5k LUTs

### 10 GigE Resource Count (128-bit )

Vivado 2014.4 targeting XC7Z045

- Full stack (UDP and 2 TCP engines) ~30k LUTs
- For each additional TCP engine ~10k LUTs



## Fraunhofer HHI is

Founded in 1949, the German Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. With a workforce of over 23,000, the Fraunhofer-Gesellschaft is Europe's biggest organization for applied research, and currently operates a total of 67 institutes and research units. The organization's core task is to carry out research of practical utility in close cooperation with its customers from industry and the public sector.

Fraunhofer HHI was founded in 1928 and joined in 2003 the Fraunhofer-Gesellschaft as the "Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut, Today it is the leading research institute for networking and telecommunications technology, "Driving the Gigabit Society" .

## Missing Link Electronics is

We are a Silicon Valley based technology company with offices in Germany. We are partner of leading electronic device and solution providers and have been enabling key innovators in the automotive, industrial, test & measurement markets to build better Embedded Systems, faster.

Our mission is to develop and market technology solutions for Embedded Systems Realization via pre-validated IP and expert application support, and to combine off-the-shelf FPGA devices with Open-Source Software for dependable, configurable Embedded System platforms.

Our expertise is I/O connectivity and acceleration of data communication protocols, additionally opening up FPGA technology for analog applications, and the integration and optimization of Open Source Linux and Android software stacks on modern extensible processing architectures.