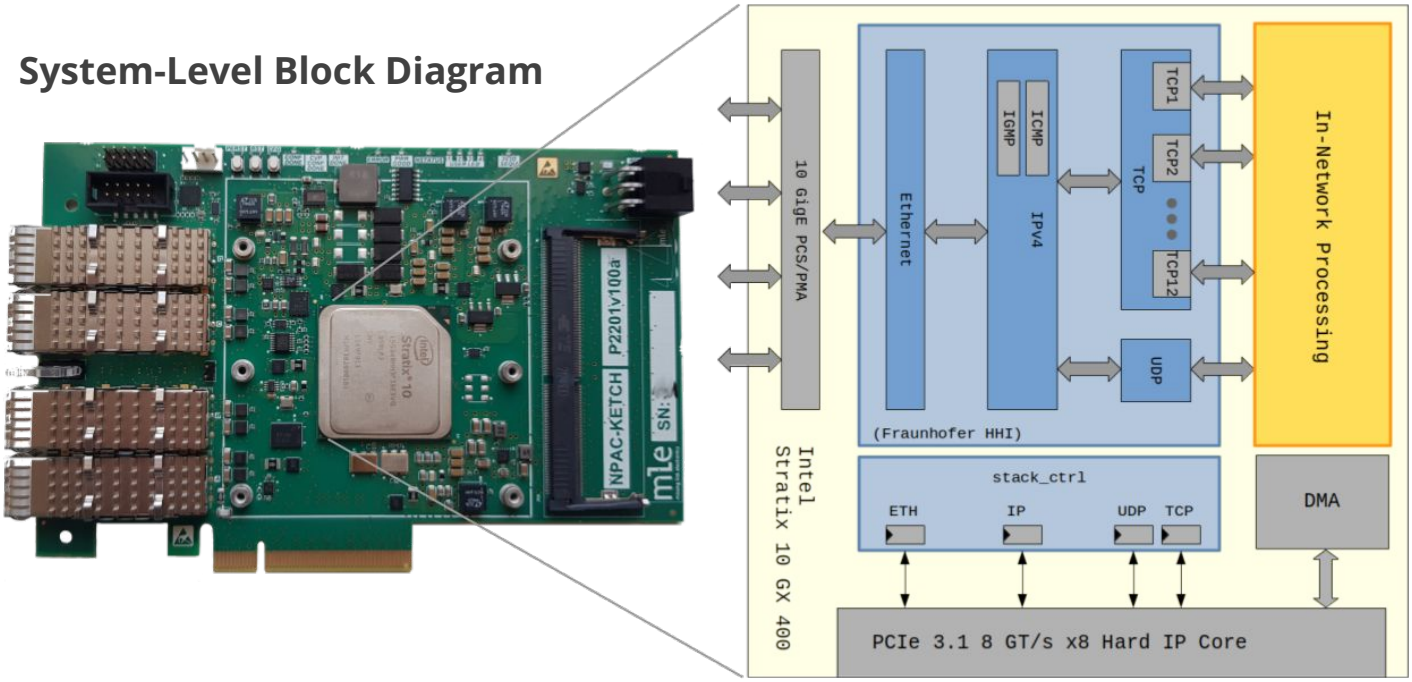
NPAC-40G: A Cost-Efficient PCIe Network Protocol Accelerator Card

MLE has partnered with Fraunhofer HHI to provide the industry-proven TCP/UDP/IP Network Protocol Acceleration Platform (NPAP) in form of NPAC, a PCIe **N**etwork **P**rotocol **A**ccelerator **C**ard with quad-port 10G Ethernet. NPAC-40G implements reliable high-bandwidth low-latency TCP/UDP/IP transport plus Linux PCIe stream device drivers and, optionally, can run customizable In-Network Processing on the integrated FPGA subsystem.

System-Level Block Diagram



Benefits

- 40 Gbps Source-to-Sink Data Transport
- Full Accelerator to fully offload the CPU
- Cost-Efficient, Customizable, Ready-to-Run

Key Features

- FHHL PCIe Card
- PCIe 3.1 x8 (~60 Gbps bandwidth)
- 4x 10 Gigabit Ethernet via SFP+
- Intel Stratix 10 GX 400 FPGA
- IETF 1122 TCP/UDP/IP Stack from FhG HHI
- IPv4 with ICMP, IGMP, DHCP, ARP
- In-Network Processing Custom User Logic
- Corundum.io MQNIC (optional)
- IEEE 802.1AS PTPv2 (optional)
- IEEE 802.1Qav 802.1Qbv Traffic Shaping

Deliverables

- Pre-configured PCIe Card, ready-to-run
- Linux device drivers (GPL sources)
- FPGA Design Project with NPAP design license for adding Custom User Logic (optional)
- Application-specific expert design services

Contact Information

- MLE USA: San Jose, CA
  +1-408-475-1490
  sales-web@MLEcorp.com
- MLE Germany: Neu-Ulm
  +49-731-141149-0
  sales-web@MLEcorp.com

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Application Use Cases

- FPGA-Based SmartNIC with TCP/IP “Full Acceleration”
- Low-Latency Time-Sensitive Networking (TSN) UPF Accelerator & NIC
- 40 GigE Network Spy, NetFilter, DPI
- 40 GigE SD-WAN Accelerator with Traffic Shaping
- High-Speed Sensor Data Acquisition and Replay
- Customizable Camera Frame Grabber for 4x 10 GigEVision
- Data-in-motion processing and streaming between networked Edge devices / Servers
- Lossless, Gapless Data Recording onto Network-Attached Storage (NAS)

Technical Specification

Total Electrical Load & Thermal	60 W, 50 W TDP passive cooling front-to-back
Form Factor	PCI-SIG CEM Rev 3.0 FHHL
Key Interfaces	4x SFP+ (10 GigE each) and PCIe 3.1 8 GT/sec x8
On-Board Memory	FPGA-attached DDR4 DRAM via SO-DIMM
Network Function Support	IETF 1122 TCP/UDP/IP plus Linux 4.18 and 5.10
Performance Metrics	128 bit wide bi-directional data paths with AXI4-Stream interfaces TCP/UDP/IP processing at full 40 Gbps line rate Door-to-door latency of 656 ns for 160 Bytes

Fraunhofer Heinrich-Hertz-Institute (HHI)

Founded in 1949, the Fraunhofer-Gesellschaft is the world’s leading applied research organization and currently operates 75 institutes and research institutions throughout Germany. The majority of the organization’s 29,000 employees are qualified scientists and engineers, who work with an annual research budget of 2.8 billion euros.

Fraunhofer HHI was founded in 1928 and joined in 2003 the Fraunhofer-Gesellschaft as the "Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut„ Today it is the leading research institute for networking and telecommunications technology, “Driving the Gigabit Society”.

Missing Link Electronics (MLE)

We are a Silicon Valley based technology company with offices in Europe and Asia.

Over the last decade we have become experts in accelerating software-rich system stacks via offloading CPUs using so-called Domain-Specific Architectures for computing. To implement we make heavy use of heterogeneous processing devices such as FPGAs which we program using C++/C/SystemC as well as VHDL and Verilog HDL.

Together with our EMS partners we offer high-performance networking and compute systems and solutions as well as licensable system stacks for adaptable compute platforms. We complement this with our expert system design services rooting in our long and deep partner relationships with FPGA vendors AMD/Xilinx and Intel.

www.missinglinkelectronics.com
+1-408-475-1490
+49-731-141149-0