Design Choices for FPGA-based SoCs When Adding a SATA Storage

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Motivation for SATA Storage for FPGA based SoCs

- ARM Cortex A9MP CPUs: fast enough to run rich OS and software
- Wide range of applications require I/O and signal processing flexibility
  - Data-Logging
  - Test & Measurement
  - Advanced Driver Assist Systems (ADAS)
  - Telematics
  - Machine Visioning
  - Broadcasting Applications
- FPGA based SoC a flexible and cost efficient alternative to embedded PCs

“Leave Your PC Behind!”

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www.missinglinkelectronics.com
## Storage Solutions for FPGA based SoCs

<table>
<thead>
<tr>
<th>FPGA Design Requirements</th>
<th>USB Thumbdrives</th>
<th>Compact Flash</th>
<th>SD Cards</th>
<th>SSD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>USB 2.0 OTG built-in into most devices</td>
<td>3rd party IP core with parallel I/O; needs many FPGA pins</td>
<td>SDIO built-in into most devices</td>
<td>3rd party IP core, needs Gigabit transceivers</td>
</tr>
<tr>
<td>Flexibility</td>
<td>Consumer driven, plenty of devices available</td>
<td>Less often used, past it’s prime</td>
<td>Consumer driven, plenty of devices available</td>
<td>Consumer driven, plenty of devices available, future proof</td>
</tr>
<tr>
<td>Capacity</td>
<td>Typ. 16 GB</td>
<td>Typ. 64 GB</td>
<td>Typ. 64 GB</td>
<td>&gt;256 GB</td>
</tr>
<tr>
<td>Performance</td>
<td>30 MB/s</td>
<td>133 MB/s</td>
<td>&lt; 100 MB/s</td>
<td>&gt; 400 MB/s</td>
</tr>
<tr>
<td>Design Cost</td>
<td>No extra cost</td>
<td>Extra cost of 3rd party IP core, needs extra FPGA resources</td>
<td>No extra cost</td>
<td>Extra cost of 3rd party SATA AHCI IP core, needs extra FPGA resources</td>
</tr>
</tbody>
</table>
Trends for Solid State Drives

Average HDD and SSD prices in USD per gigabyte

Data sources: MiKoMo, Gartner, and Pingdom (December 2011)
SATA Backgrounder


<table>
<thead>
<tr>
<th>Official naming</th>
<th>In-official naming</th>
<th>Netto-Datarate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial ATA 1.5 Gbit/s</td>
<td>SATA I</td>
<td>150 MB/s</td>
</tr>
<tr>
<td>Serial ATA 3.0 Gbit/s, SATA Revision 2.x</td>
<td>SATA II, SATA-300</td>
<td>300 MB/s</td>
</tr>
<tr>
<td>Serial ATA 6.0 Gbit/s, SATA Revision 3.x</td>
<td>SATA III, SATA-600</td>
<td>600 MB/s</td>
</tr>
</tbody>
</table>

Performance Aspects

- Bandwidth (MB per second)
  - read vs. write, sequential vs. random access, compression or not
- IOPs (I/O operations per second)
  - Defined by Flash cell types, host and device controller
By default, one Frame Information Structure (FIS) packet gets transferred after the other using standard Direct Memory Access (DMA).

With Native Command Queuing (NCQ), FIS packets can be transferred in an interleaving fashion using First-Party DMA (FPDMA).
Importance of FPDMA / NCQ
## SATA Functionality Layers

<table>
<thead>
<tr>
<th>Functionality Description</th>
<th>Design Aspect</th>
</tr>
</thead>
<tbody>
<tr>
<td>User Programs</td>
<td>Application software development</td>
</tr>
<tr>
<td>Block Device Layer (/dev/sdX)</td>
<td>GNU/Linux Operating System</td>
</tr>
<tr>
<td>Device layer</td>
<td>Custom Device Driver</td>
</tr>
<tr>
<td>Application layer</td>
<td>SATA AHCI IP Core</td>
</tr>
<tr>
<td>Transport layer</td>
<td>Built-in FPGA high-speed Gigabit Transceivers</td>
</tr>
<tr>
<td>Link layer</td>
<td>Phv layer</td>
</tr>
</tbody>
</table>
Architecture Option 1: Built-in PL330 DMA Controller

Full functionality but very limited performance without hardware support for NCQ

Scatter-Gather support needs software work for Linux
Significantly better performance, but does not “max out SSD”!

SSDs' internal structure demands NCQ for full R/W performance
Close to “max out SSD”!

Depending on application, bottleneck is in software (IOPS)

This can be caused by too many IRQs
Command Completion Coalescence (CCC) to reduce interrupt and command completion overhead in heavily loaded systems [Serial ATA AHCI 1.3]

- Frees up CPU
- Increases #IOPs
- ➡️ Functionality of 3rd party SATA AHCI IP core

Striping over multiple SATA links into multiple SSDs (a.k.a. RAID-0)
- Software-RAID will **not work** due to CPU load
- ➡️ Extra functionality in 3rd party SATA AHCI IP core
Building performance storage solutions for FPGA-based SoCs is more than an IP core!

- Requires a fine-tuned micro-architecture properly integrated into the software system.
- Benefits of pre-validated FPGA subsystems.

See us at Xilinx booth Hall 1/1-205