# Low-Latency Solutions for Storage-Hungry Embedded Applications

## “Flash-on-Ethernet?”

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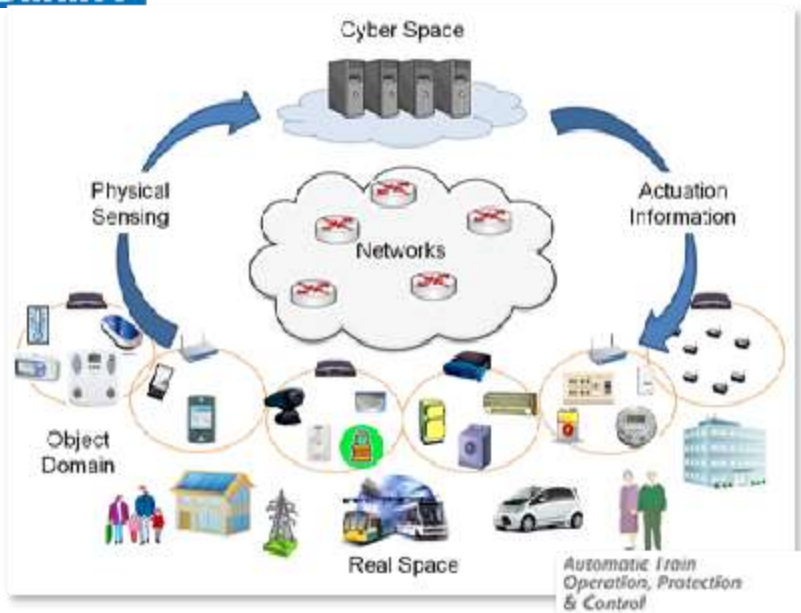
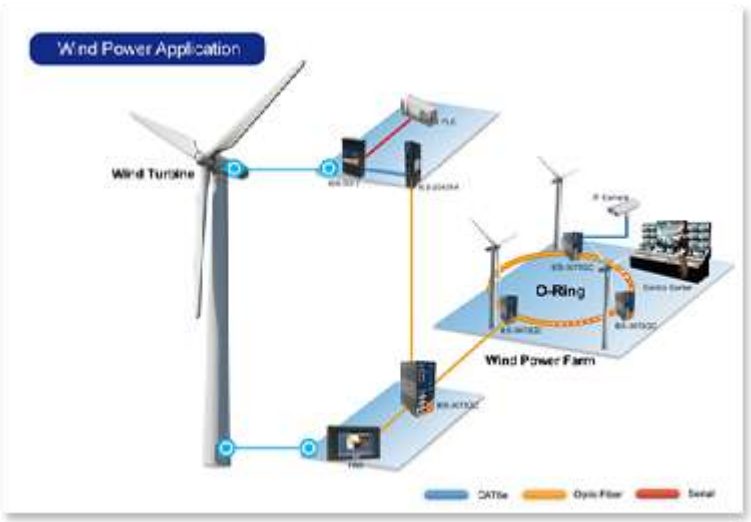
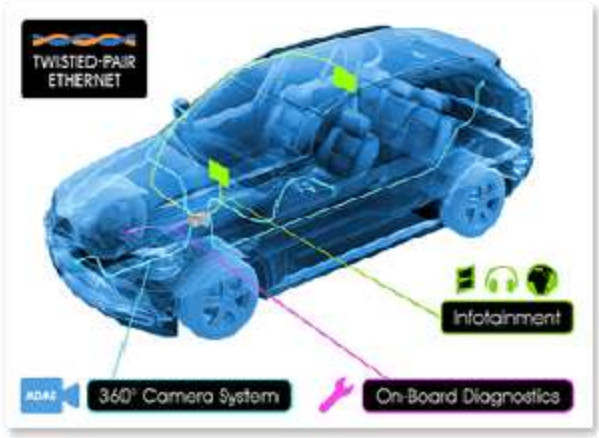
Dr. David Boggs, MLE
Dr. Ulrich Langenbach, Fraunhofer HHI
Dr. Peter Gregorius, Fraunhofer HHI

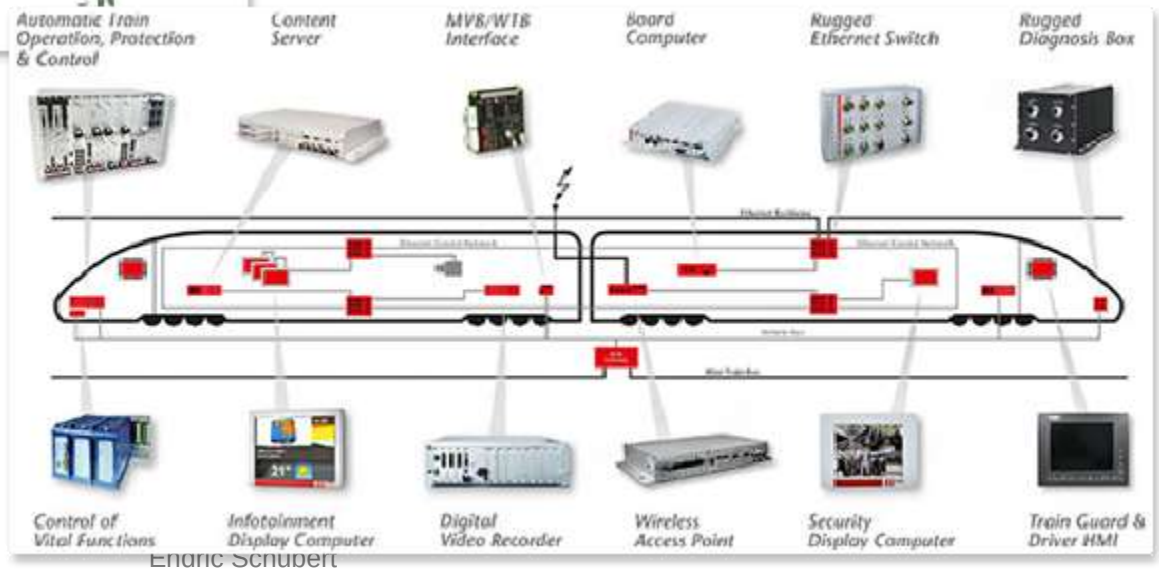
**MLEcorp.com/FoE**

# Systems-of-Systems





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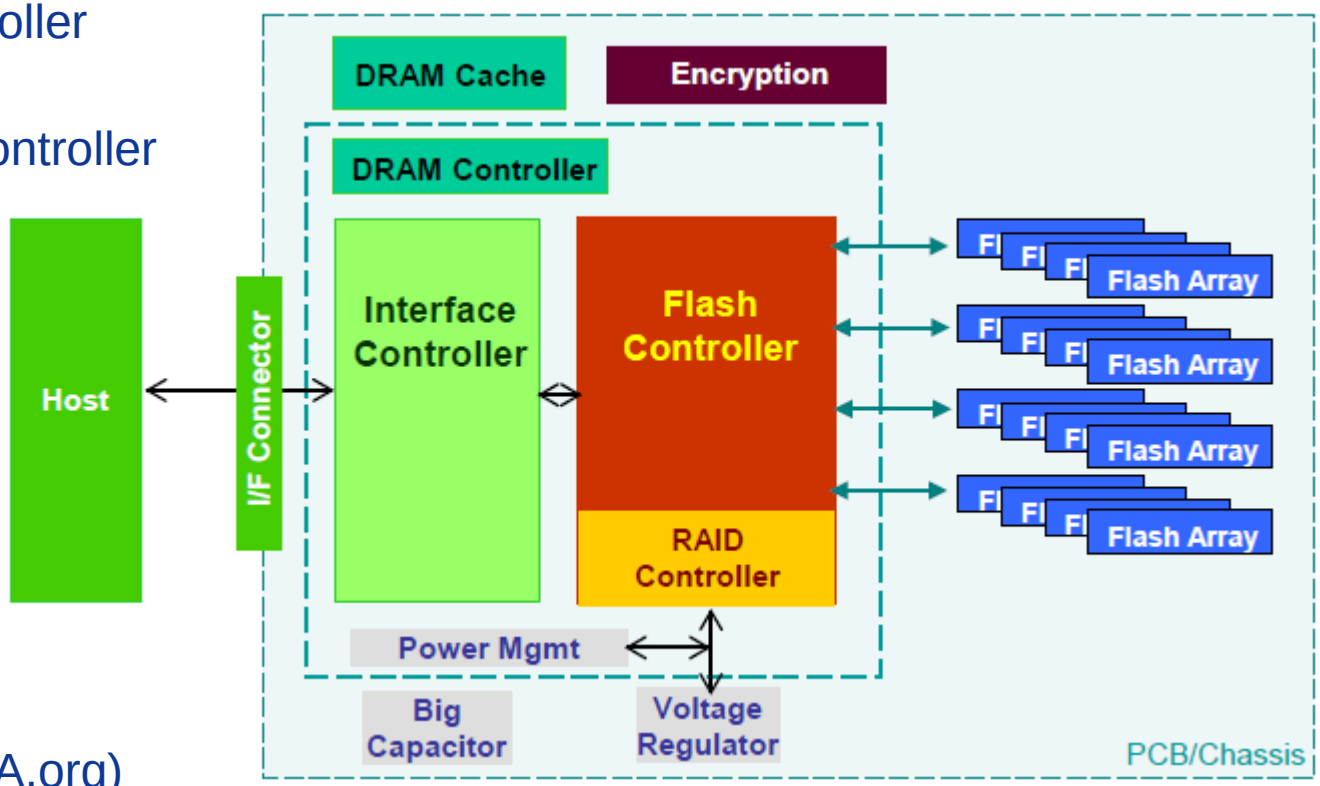
# SSD Architecture Overview

- Others:
  Flash Controller
- MLE:
  Interface Controller




(Courtesy: SNIA.org)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# Flash-on-Ethernet

- Fast Network i/f
  - 10GbE / 40GbE
- Dependable Protocol
  - iSCSI
- Future-proof SSD i/f
  - NVMexpress




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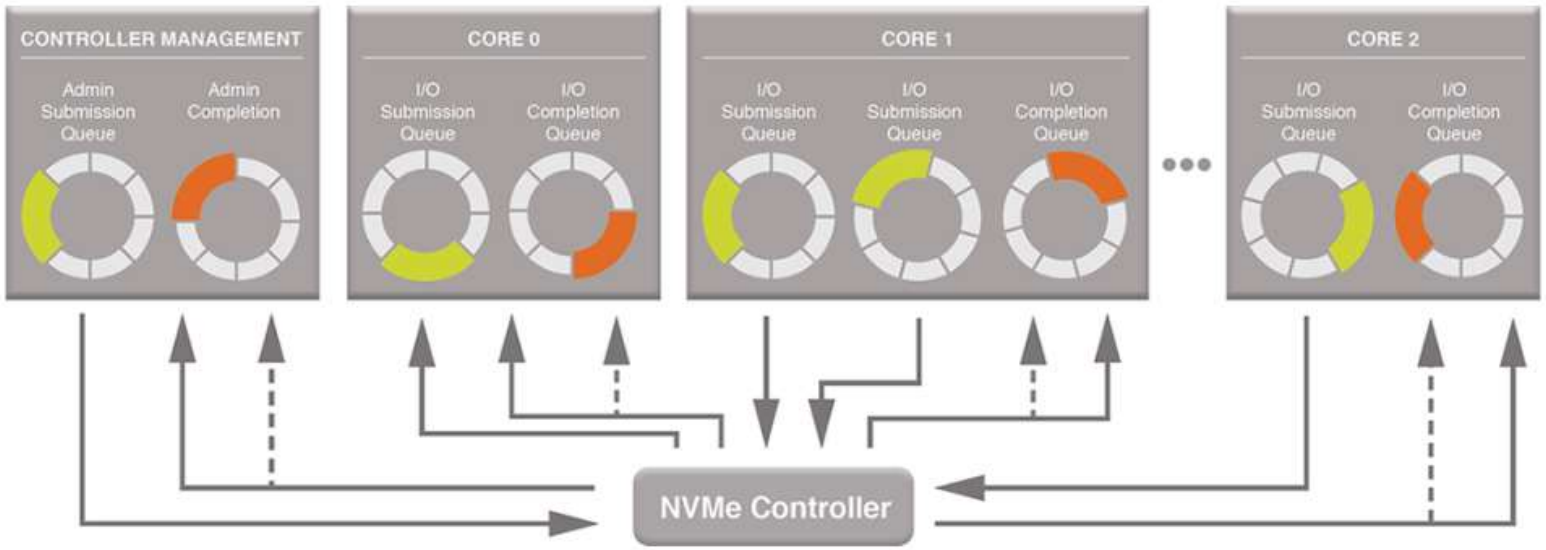
# Benefits of NVMexpress

- Built for PCIe and Flash
- Multi-Queue Facilitates Acceleration





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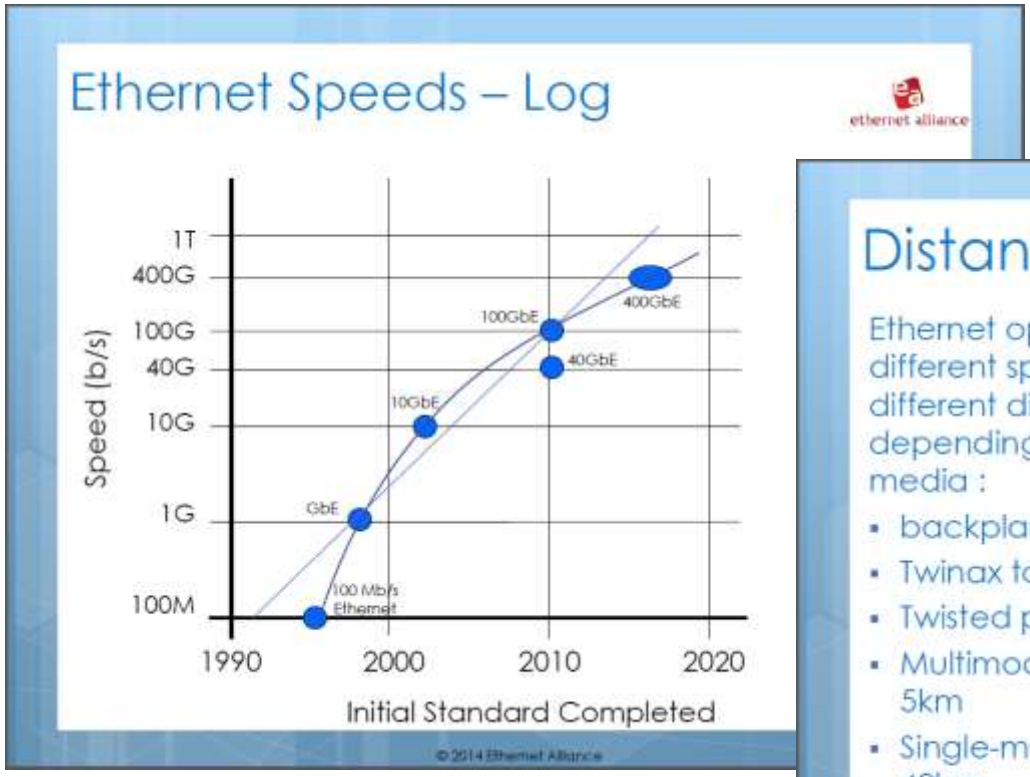
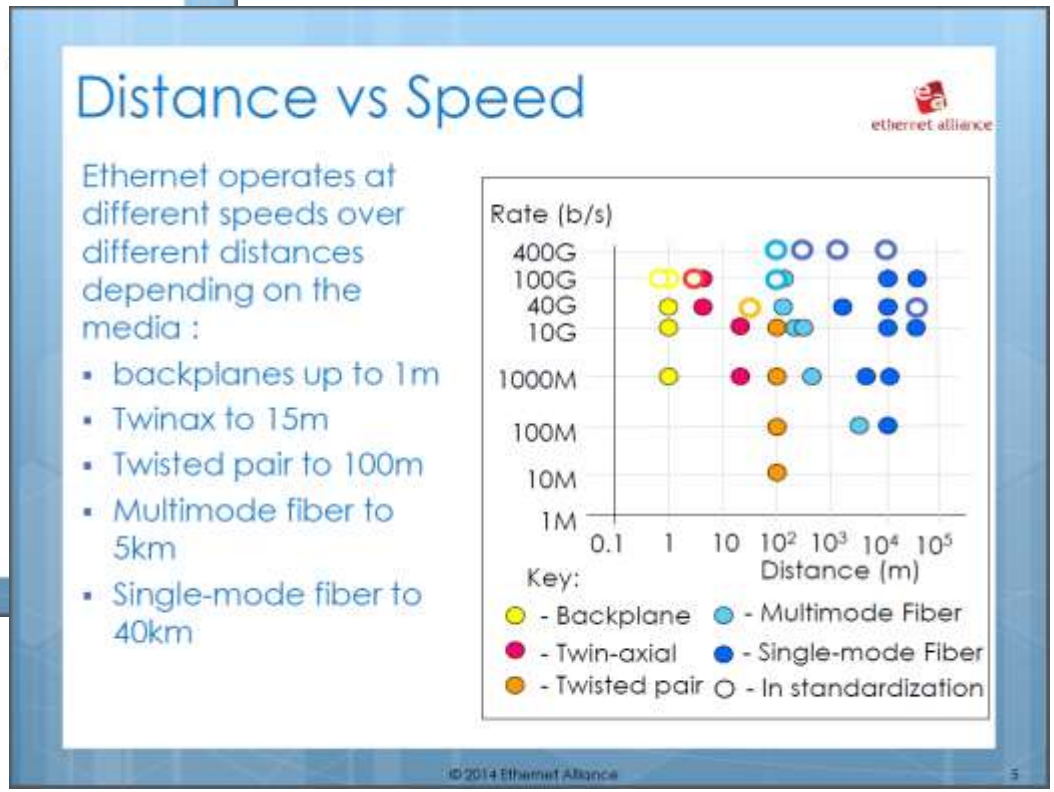
# Benefits of Ethernet

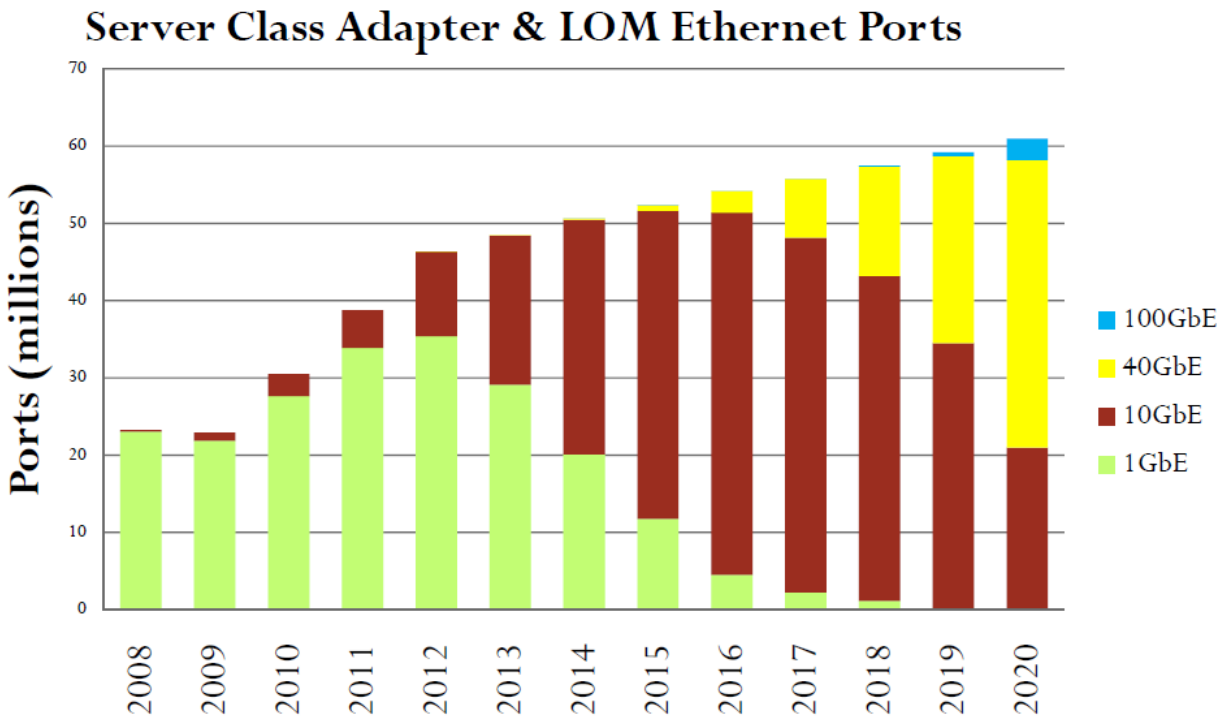



(Courtesy: Ethernet Alliance)

# Benefits of Ethernet

## Add Some History and Map it to Port Volume




Source data: Crehan Research, 2012

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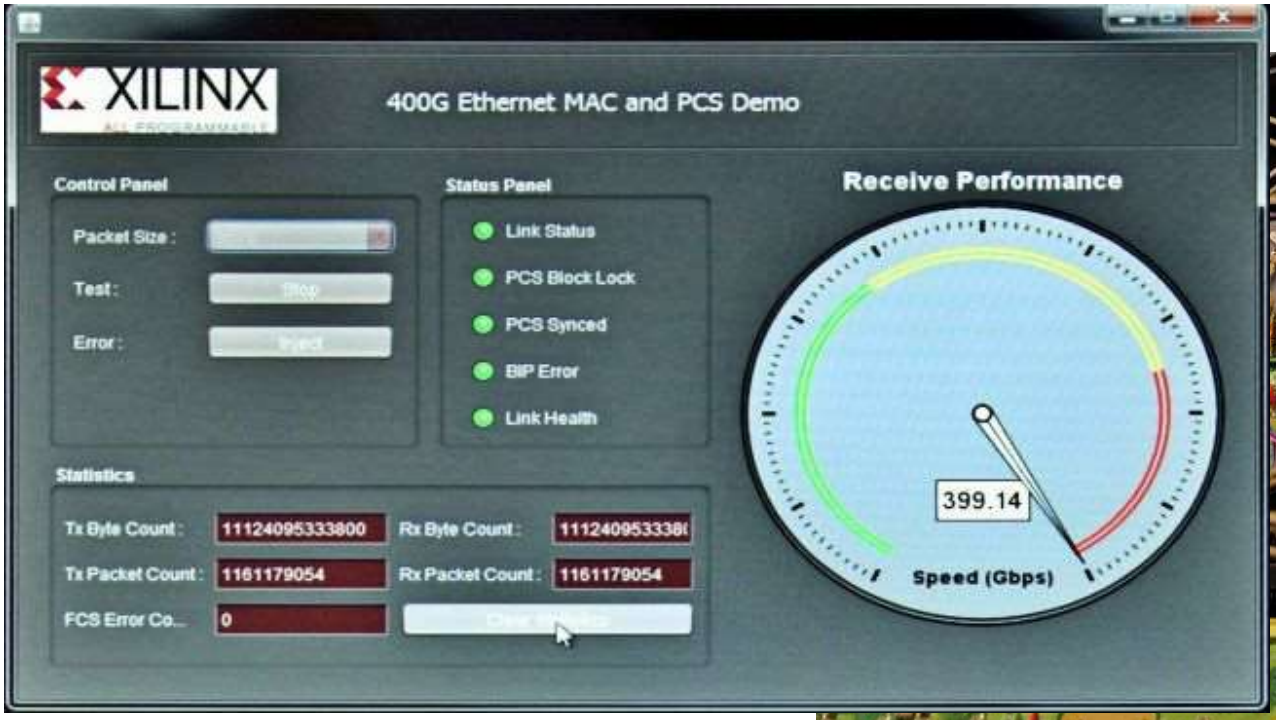
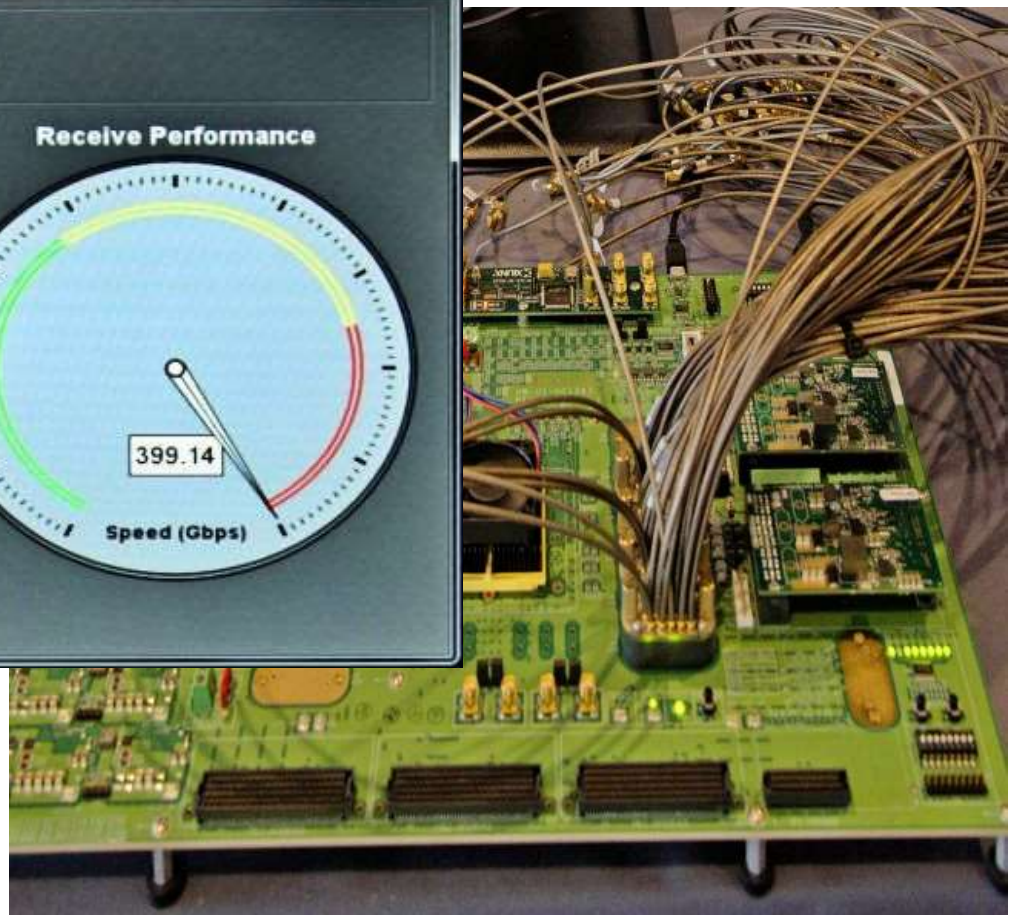
IEEE 802.3 Higher Speed Ethernet Consensus Ad Hoc

September 2012

# 400 Gigabit/s Ethernet



WDM & Next Generation Optical Networking 2014 conference in Nice, France (courtesy Xilinx)



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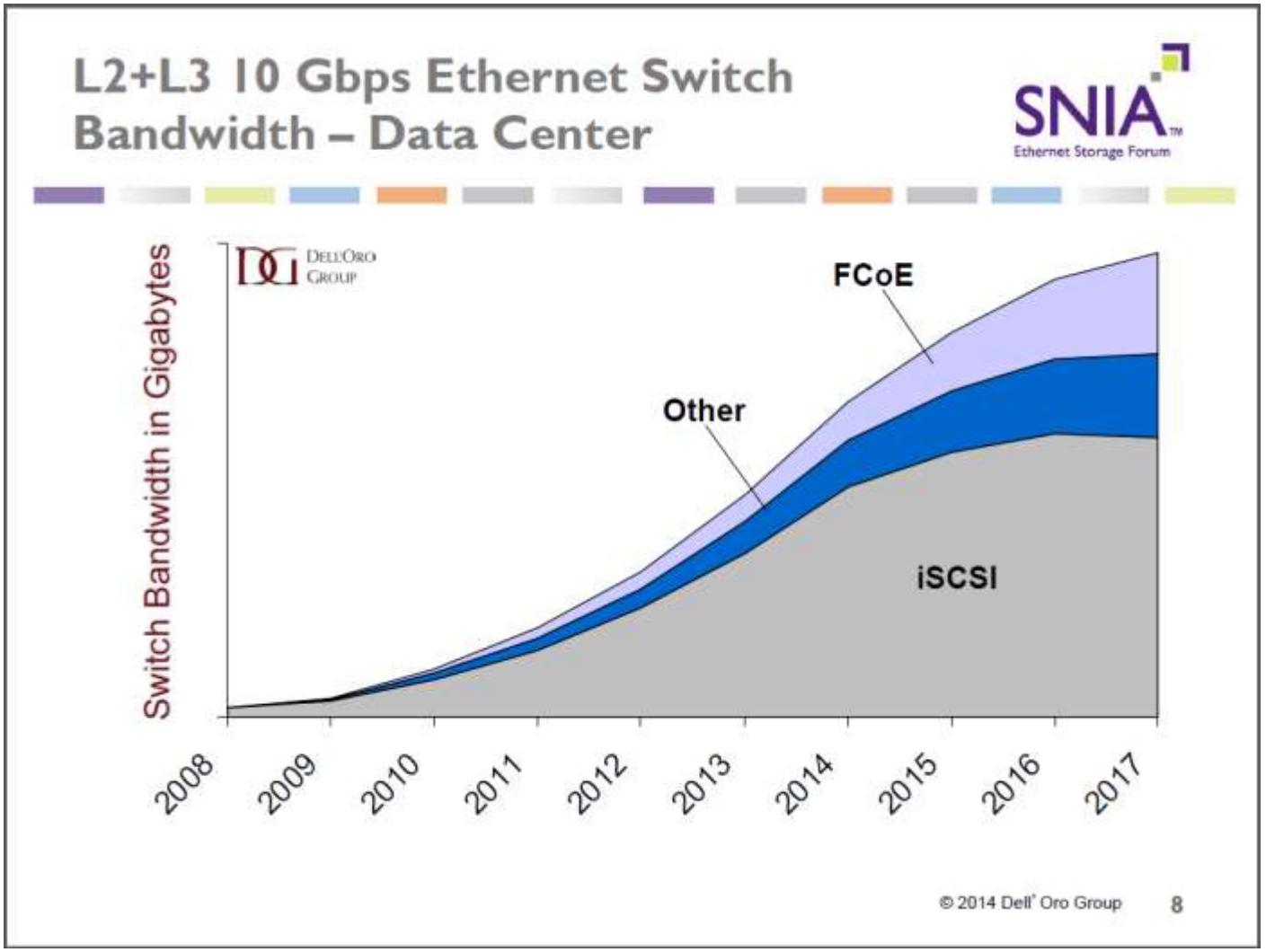
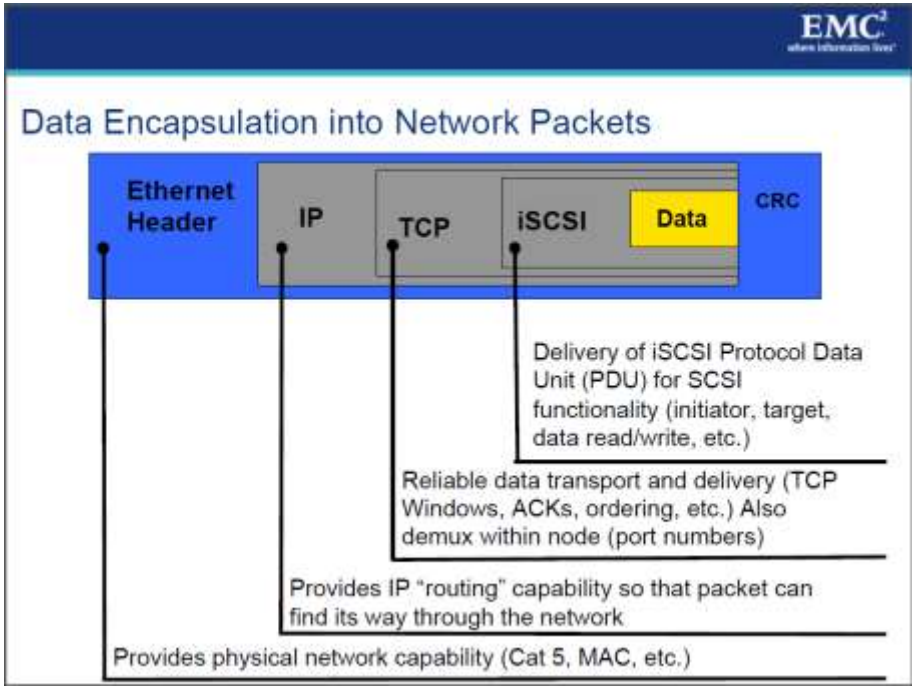
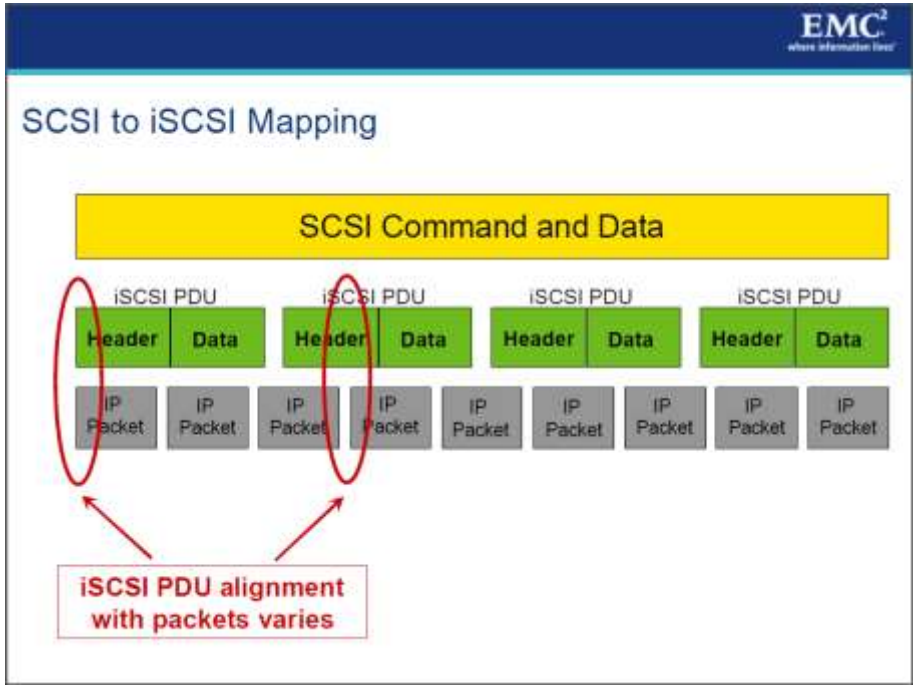
# Benefits of iSCSI



# Challenges with iSCSI

Computational complexity, Unpredictable latency





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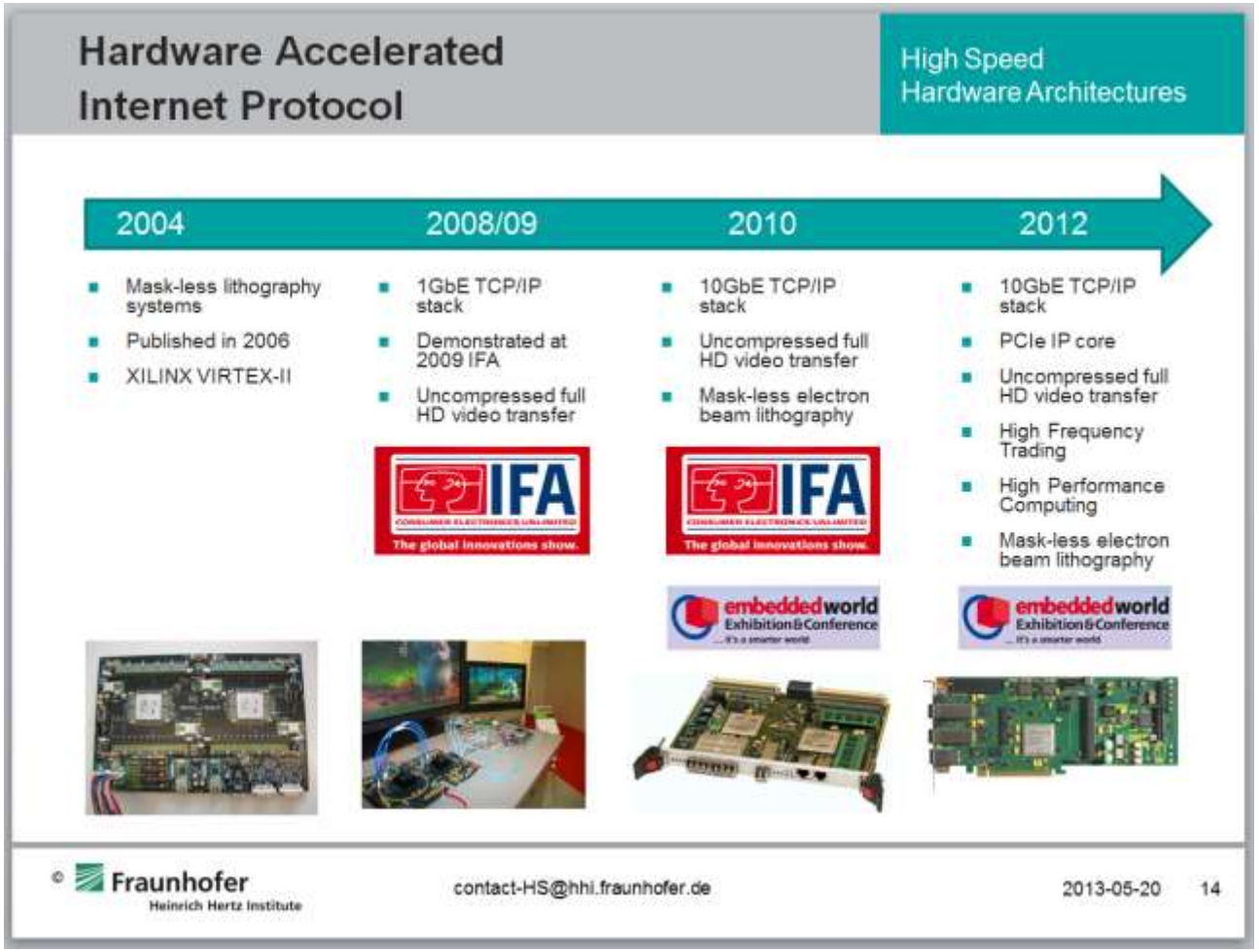
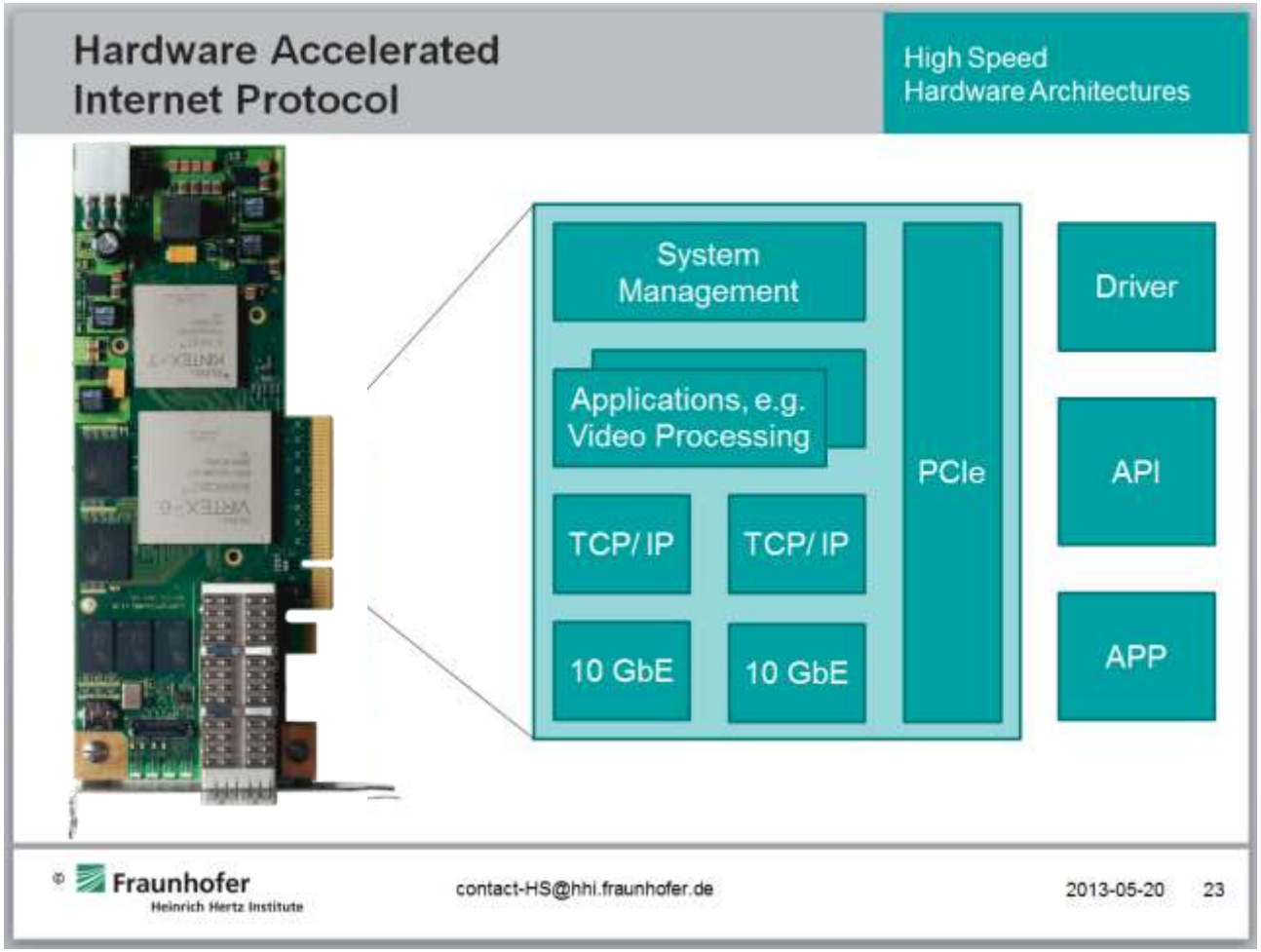
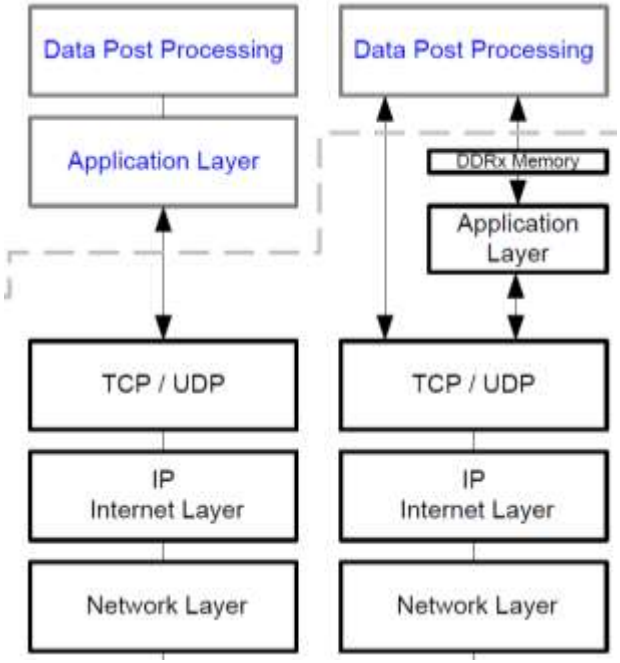
# Network Protocol Acceleration Technology from FhG HHI



# Network Protocol Acceleration Technology from FhG HHI



# Network Protocol Acceleration More Than TOE

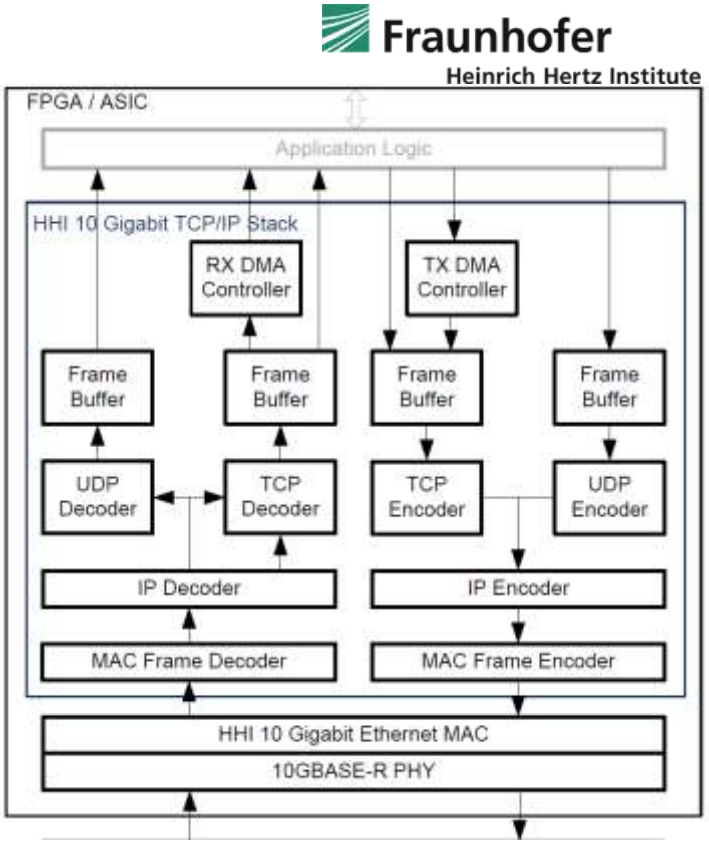



Fraunhofer HHI

- Entire TCP / UDP protocol processing inside FPGA
- Option to run Application Layer processing in HW, too!

State-of-the-Art

- Software-only
- TCP Offload Engine (TOE)
- requires CPU





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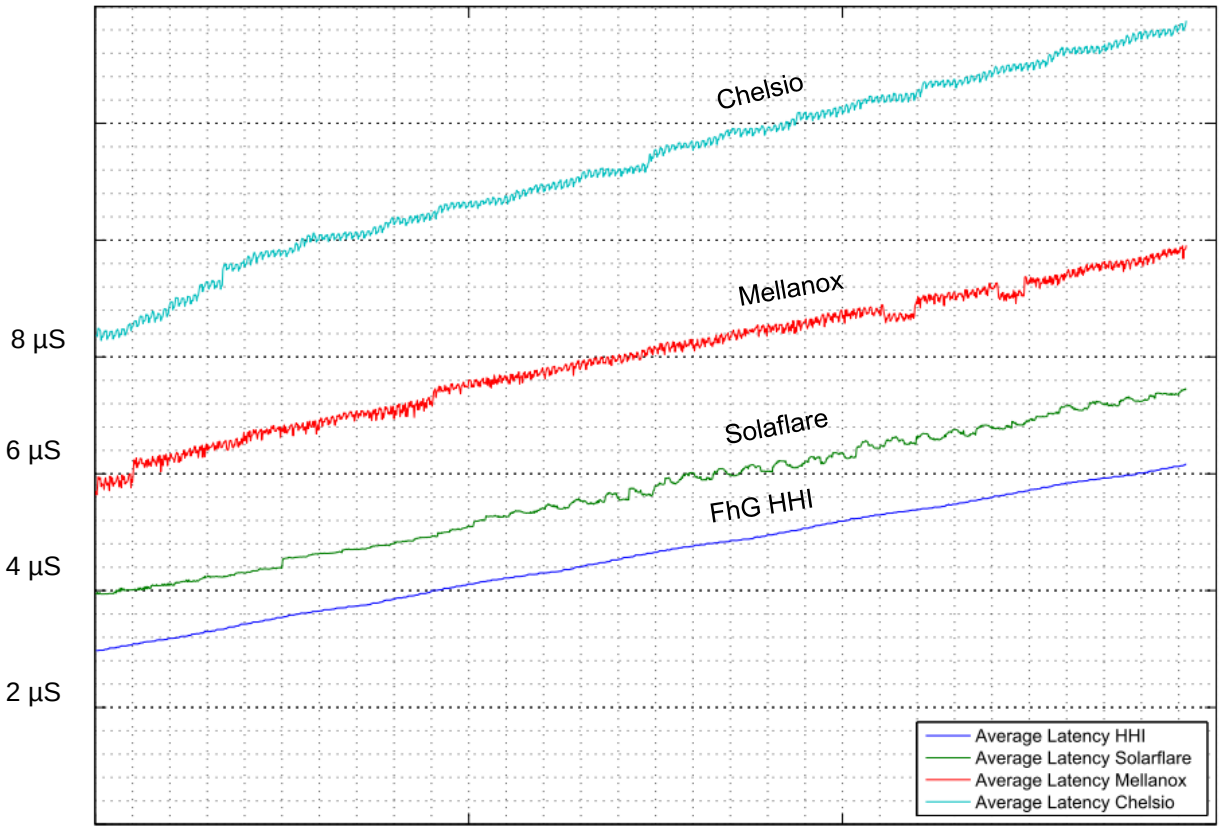
# Network Protocol Acceleration Best in Class Performance

- Stand-alone TCP/IP & UDP/IP stack
- Point-to-point 1GbE or 10GbE
- Full line rate of TPRmax = 9.5896 Gbps
- TCP R/W latency of TTR(W) ≥ 1.4 µs
- UDP R/W latency of TUR(W) ≥ 0.75 µs
- Round trip time of RTTmin ≥ 2.25 µs

(2013 benchmarking data from Fraunhofer HHI)





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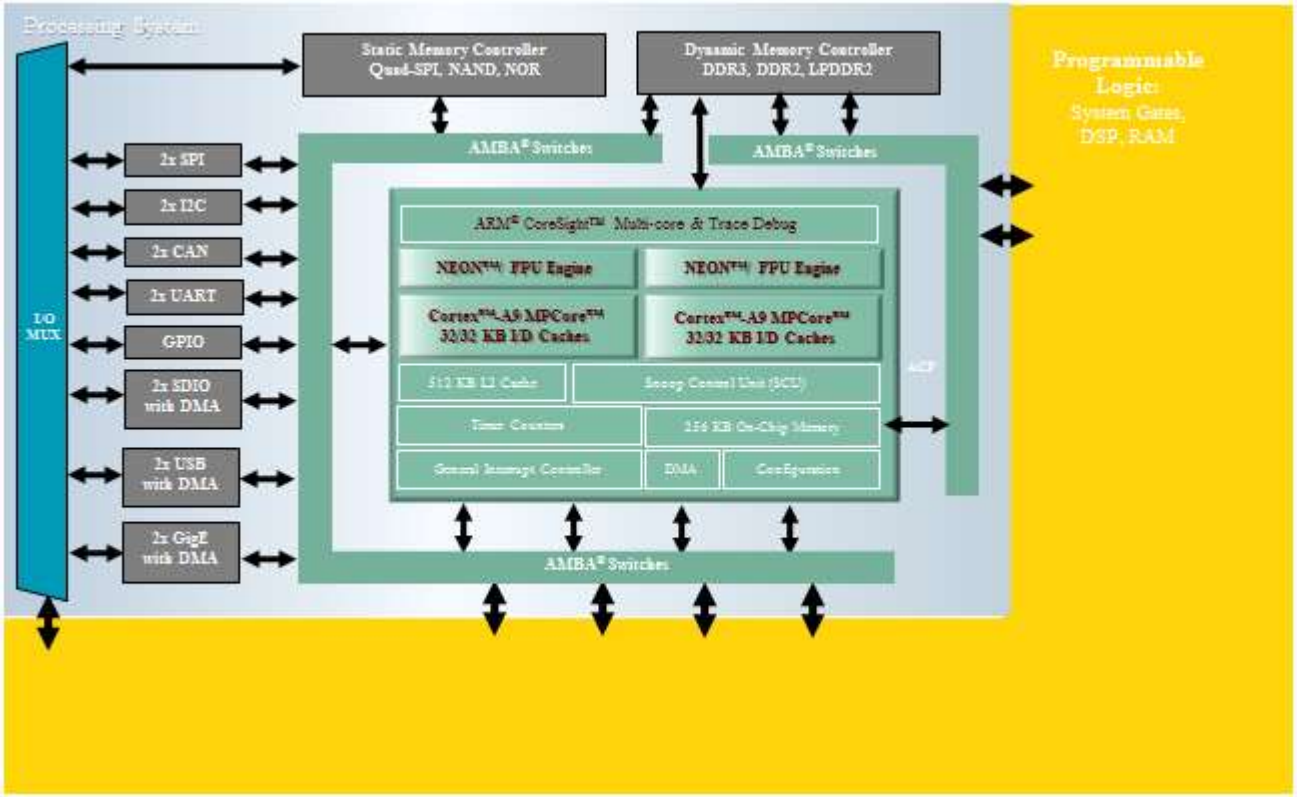
# Hardware Acceleration Enabled by Modern All-Programmable SoC

Programmable I/O

Programmable Software

Programmable Logic




"Put the processing burden where it belongs!"



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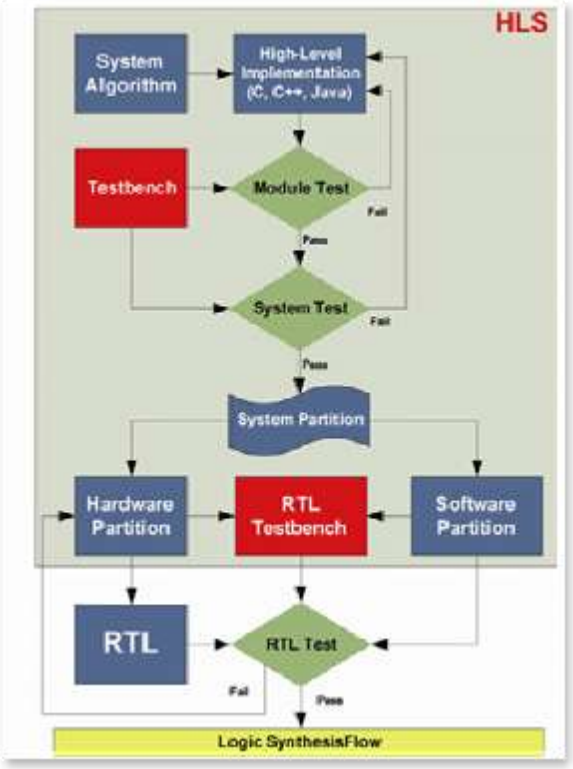
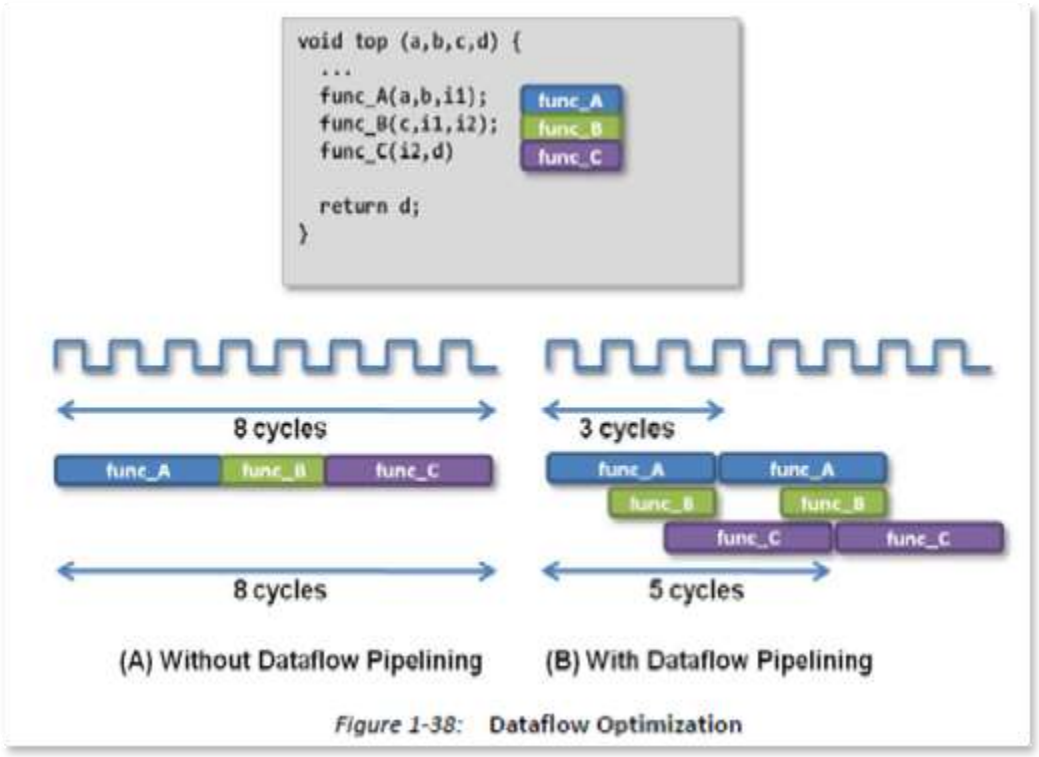
# FPGA Implementation via High-Level Synthesis




- Xilinx UG902 – Vivado Design Suite User Guide, High-Level Synthesis
- Xilinx XAPP1209 – Designing Protocol Processing Systems with Vivado HLS



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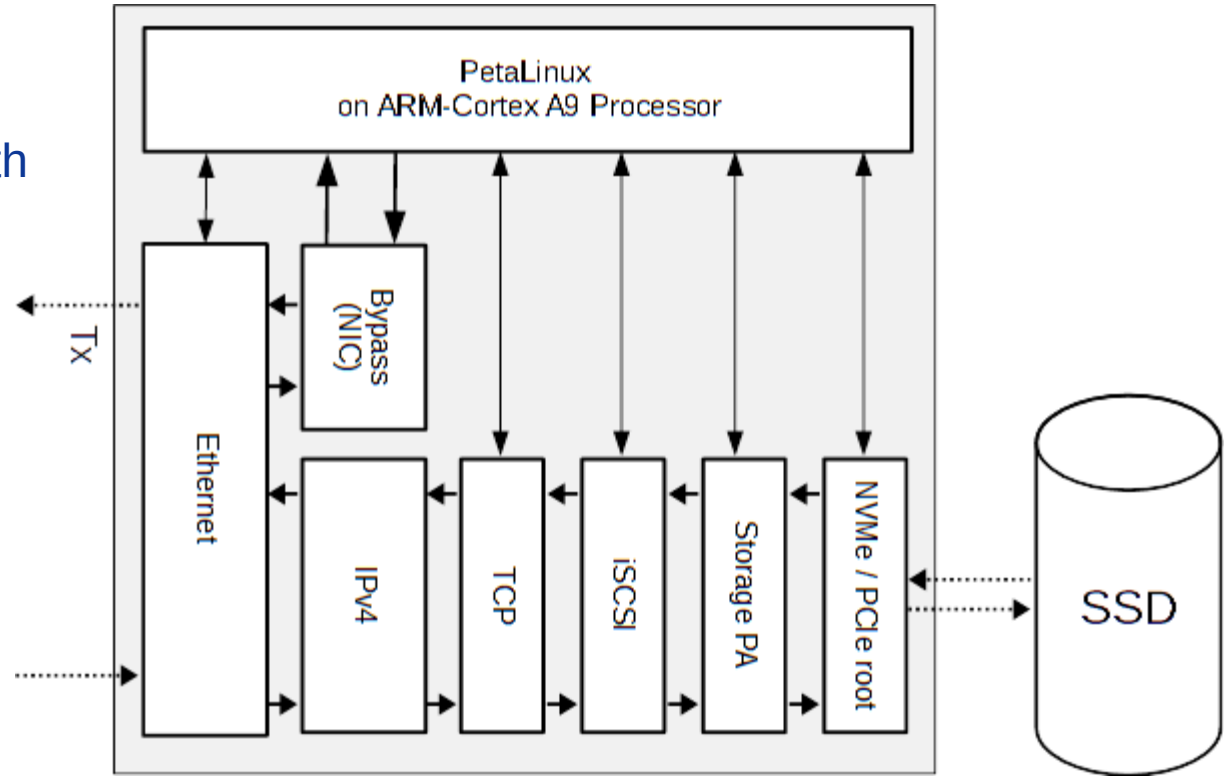
# Flash-on-Ethernet Architecture

Configurable, elastic system

Balance data rates for Latency and Bandwidth

- SSD
  - 200k IOPS
  - 800 MB/s
  - PCIe Gen2 x2
  - 10GbE
- SSD
  - 800k IOPS
  - 3 GB/s
  - PCIe Gen3 x4
  - 40 GbE



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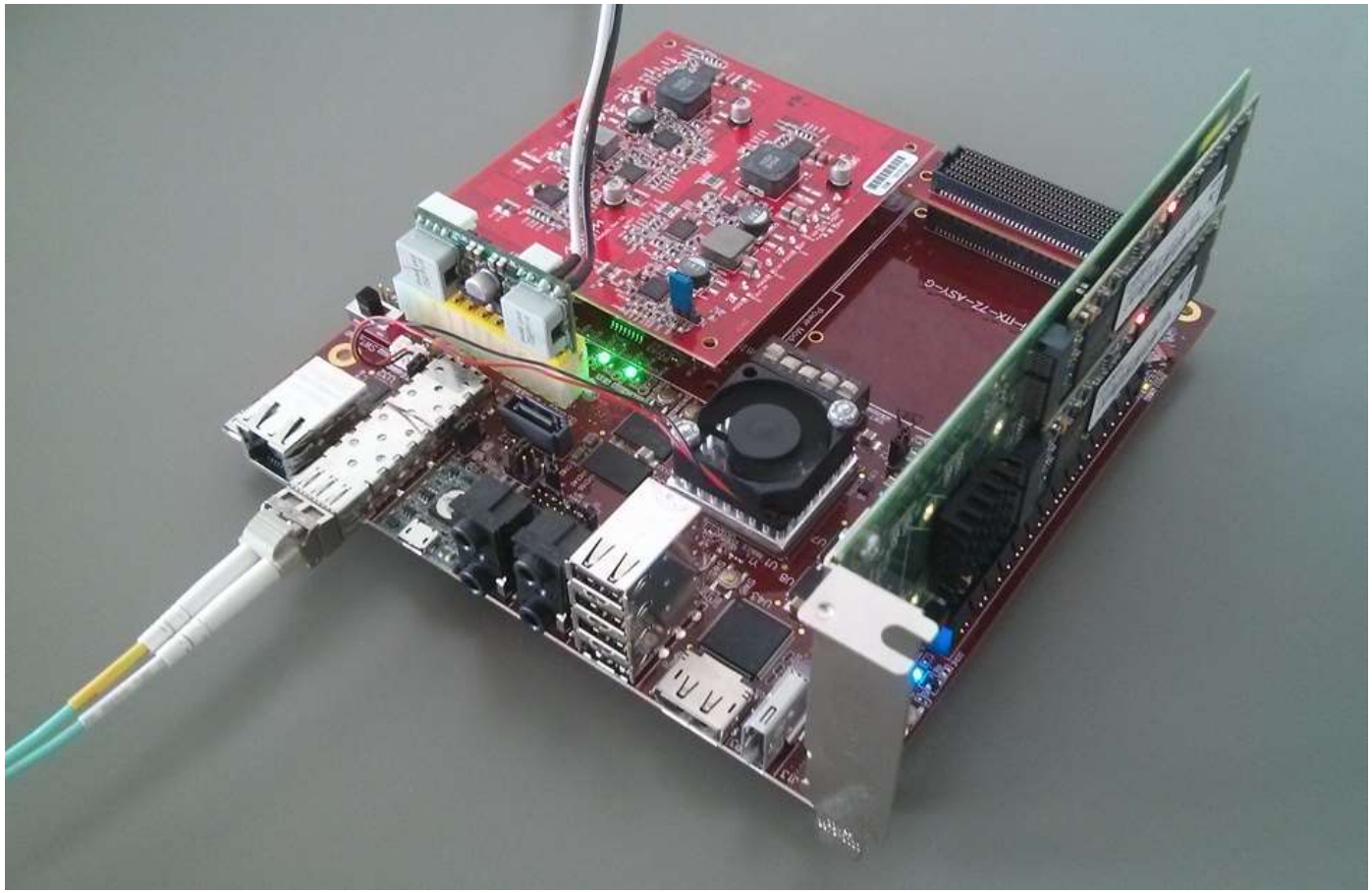
# Flash-on-Ethernet Lab Setup at MLE

- Avnet Mini-ITX
- Xilinx Zynq 7045
- PetaLinux
- AHCI SSD via PCIe
- NPAP
- 10GbE





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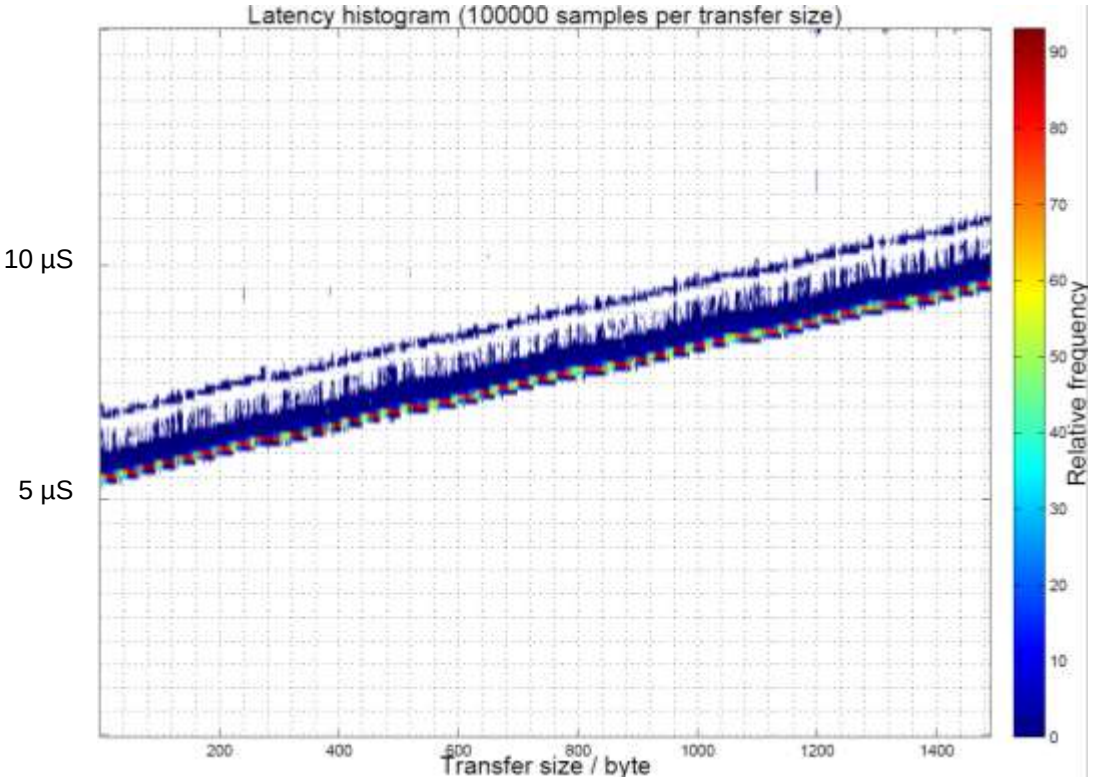
# Preliminary Results

- Good determinism
- Reasonable Latency



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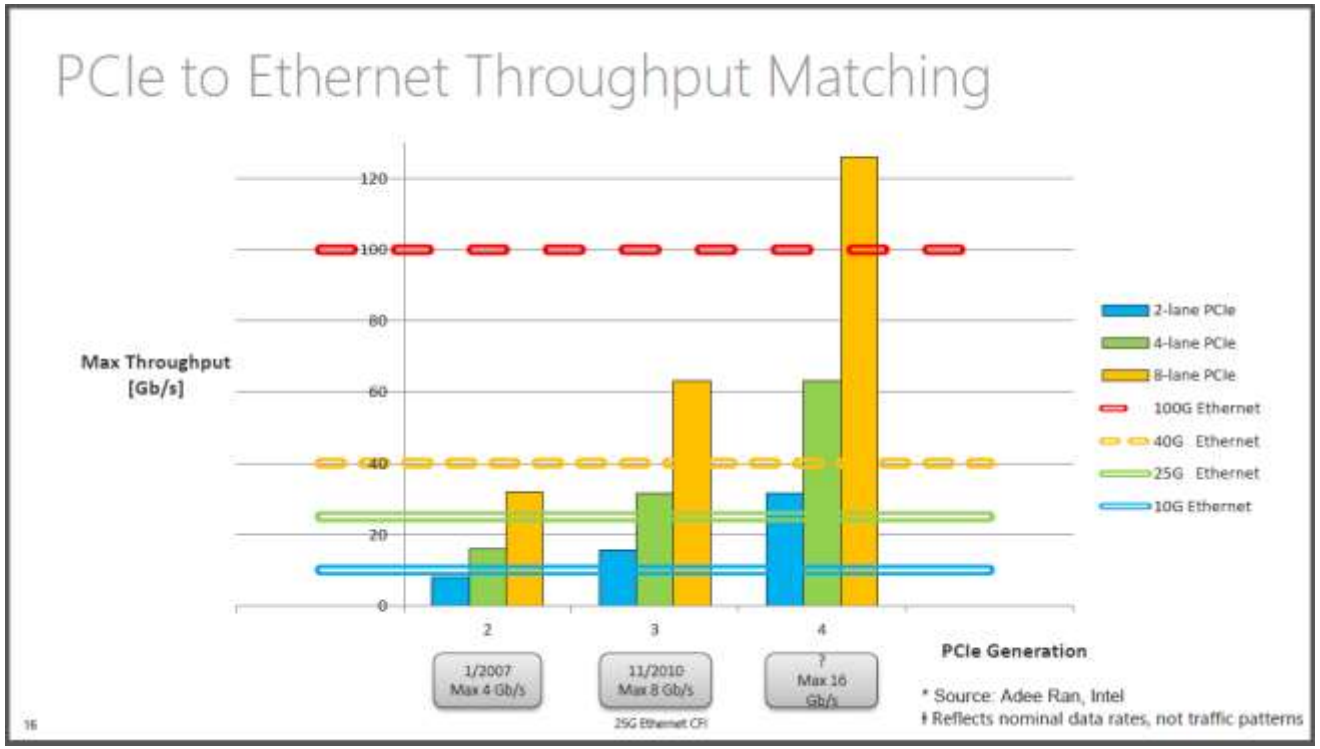
# Outlook

- Embrace Faster Ethernet: 25GbE, 40GbE




(Courtesy:
Brad Booth,
Microsoft,
25G Ethernet CFI)



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# Abstract

System-of-systems are loosely coupled Embedded Systems which greatly benefit from the high performance of modern SSD technology. Machine visioning, medical imaging, and advanced driver assist systems are among those storage-hungry applications. However, communication latency and bandwidth in between the systems have a significant impact on the overall robustness, cost and performance.

Current techniques based on fieldbuses such as CAN, Flexray, have begun to hit the bandwidth wall and are more and more replaced by multi-Gigabit Ethernet plus techniques for hardware-acceleration of networking protocol stacks.

We present a proof-of-concept implementation specifically targeted for storage-hungry System-of-systems. Integrated into a modern FPGA with multicore ARM CPUs to run Open Source Linux, single-chip solutions become possible which provide full compatibility with all relevant network and storage interface protocols and can reach userspace latencies within few microseconds.


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# Missing Link Electronics is …

We are a Silicon Valley based technology company with offices in Germany. We are partner of leading electronic device and solution providers and have been enabling key innovators in the automotive, industrial, test & measurement markets to build better Embedded Systems, faster.

Our mission is yo develop and market technology solutions for Embedded Systems Realization via pre-validated IP and expert application support, and to combine off-the-shelf devices with Open-Source Software for dependable, configurable Embedded System platforms.

Our expertise is I/O connectivity and acceleration of data communication protocols, additionally opening up FPGA technology for analog applications, and the integration and optimization of Open Source Linux and Android software stacks on modern extensible processing architectures.

MLE is a technology partner of Fraunhofer Heinrich-Hertz-Institute, a Certified Xilinx Alliance Partner, a member of the Altera Design Service Network, and an active contributor to the Open Source software ecosystem.



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# Fraunhofer HHI is…

Founded in 1949, the German Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. With a workforce of over 23,000, the Fraunhofer-Gesellschaft is Europe's biggest organization for applied research, and currently operates a total of 67 institutes and research units. The organization's core task is to carry out research of practical utility in close cooperation with its customers from industry and the public sector.

Fraunhofer HHI was founded in 1928 as "Heinrich-Hertz-Institut für Schwingungsforschung" and joined in 2003 the Fraunhofer-Gesellschaft as the "Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut„

Today it is the leading research institute for networking and telecommunications technology, "Driving the Gigabit Society" .

Fraunhofer
Heinrich Hertz Institute


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