Low-Latency Networking for Systems-of-Systems

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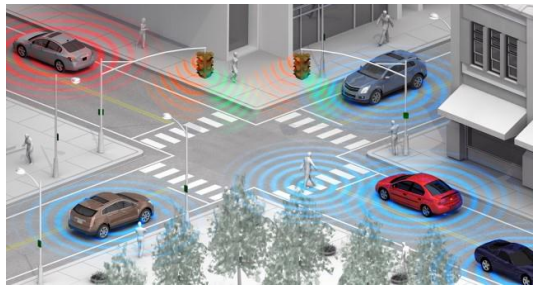
System-of-Systems

- Wikipedia: “A collection of task-oriented or dedicated systems that pool their resources and capabilities together to create a new, more complex system…”

- Cyber-Physical Systems

- Industrie 4.0

- Car-to-X



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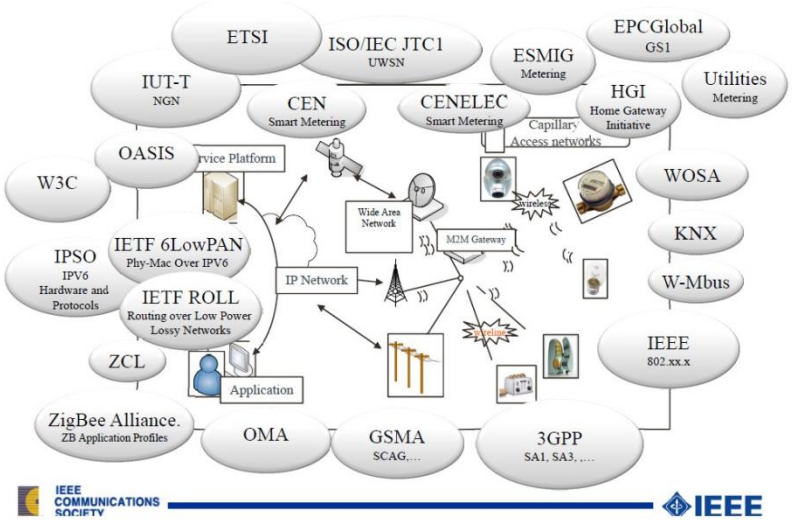
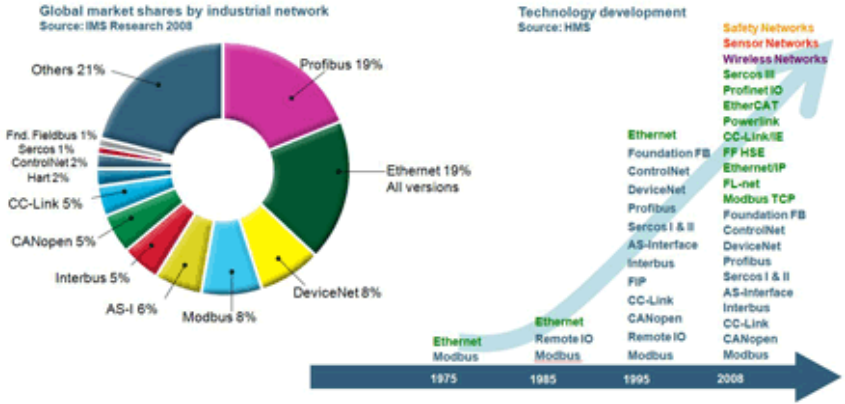
The Networking Standards “Soup”





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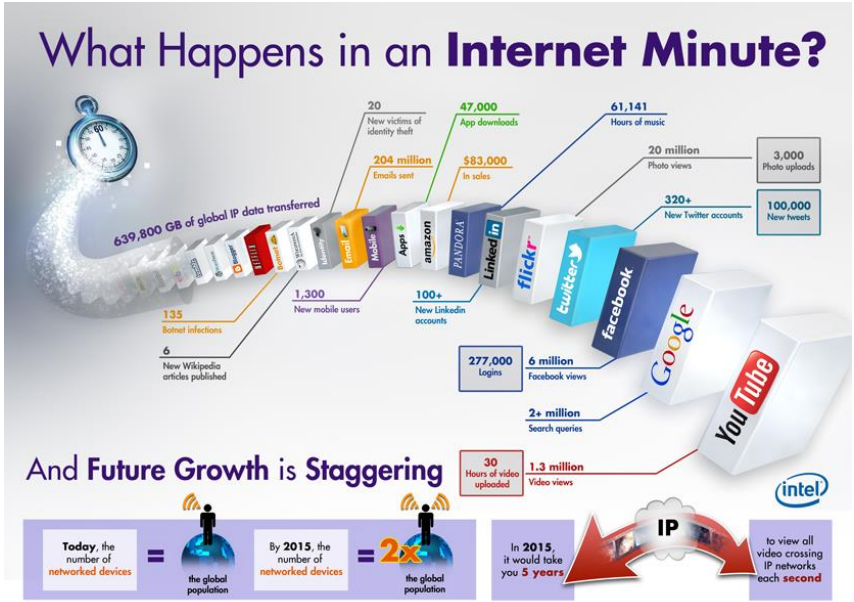
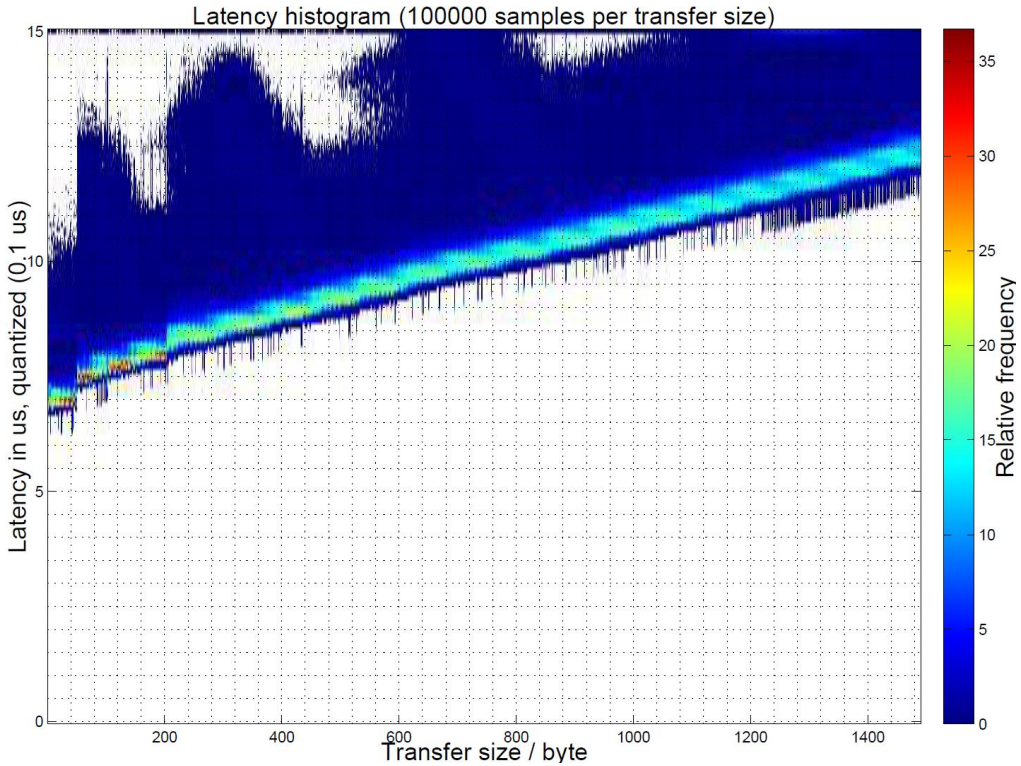
Transmission Control Protocol / Internet Protocol Suite

- The success of TCP/IP
  - Scalable
  - Reliable
  - Ubiquitous
  - Open Standards
- Great candidate for networking backbone of systems-of-systems!



Latency Aspects in TCP/IP Networking

- Many ways to measure latency:
  - Round-Trip-Time (RTT)
  - Response Time
  - Worst-Case Execution Time
- Robust distributed control systems depend on:
  - Low latency
  - Deterministic latency numbers
  - TTP – TDMA
- More important:
  latency * bandwidth



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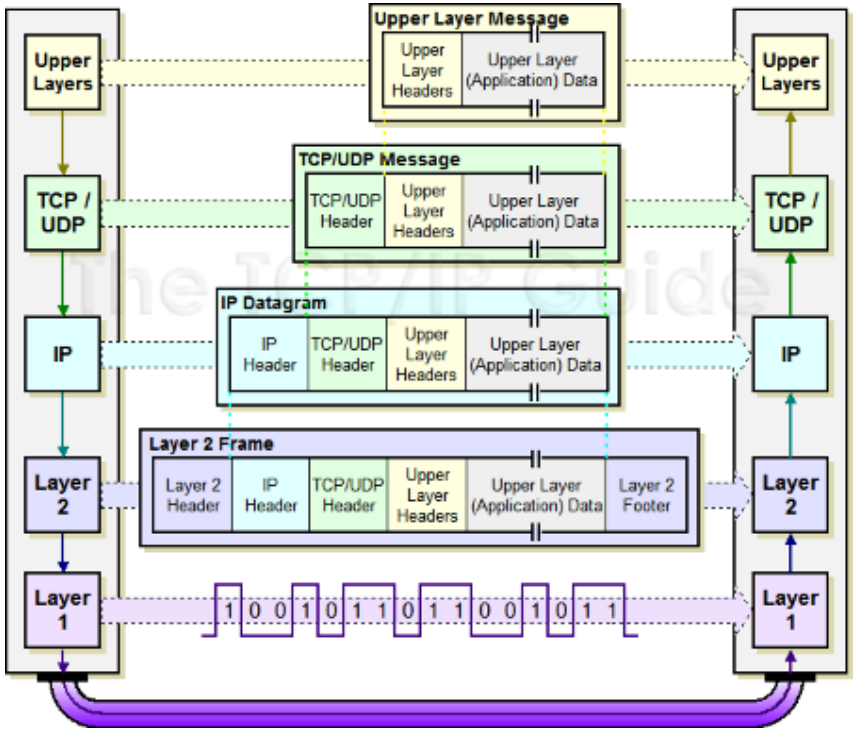
Backgrounder TCP/IP

- Layered architecture
- “Packet”-based with data segmented into Protocol Data Units (PDU)
  - TCP message – PDU at TCP layer
  - Datagram – PDU at IP layer
  - Frame – PDU at link-layer
- Communication is
  - Reliable
  - Ordered
  - Error-checked



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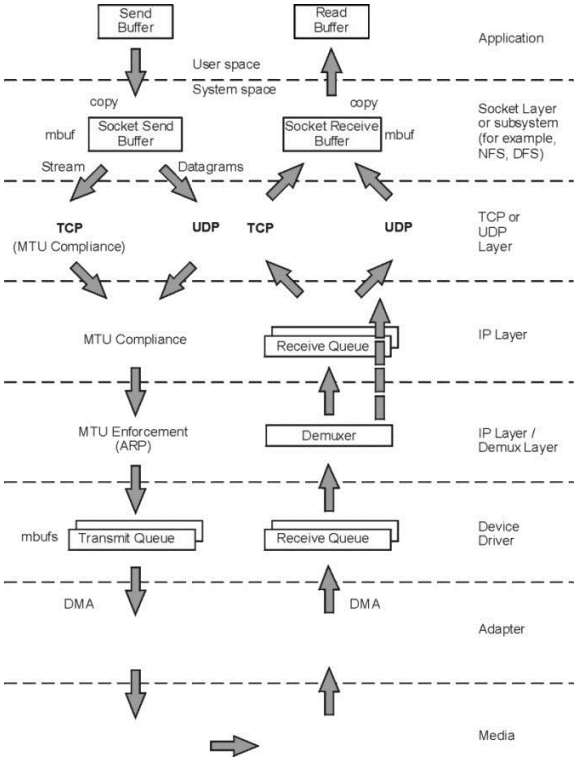
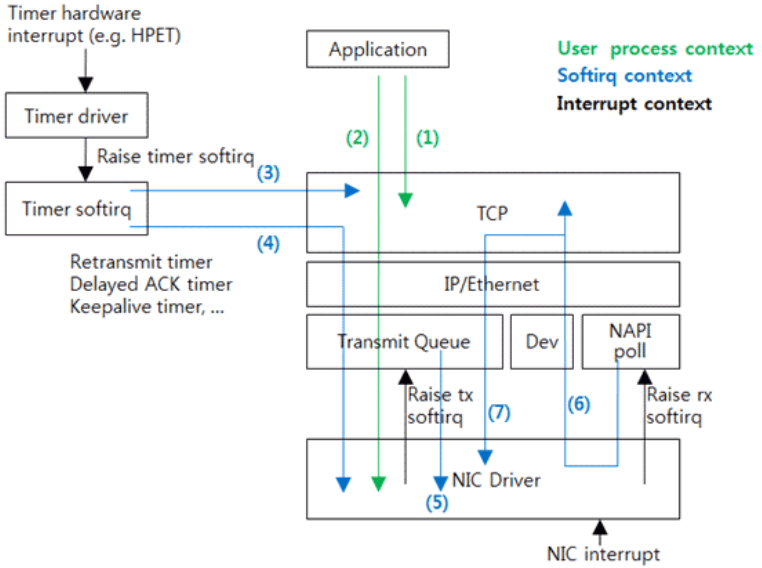
Computational Aspects of TCP/IP Processing



Transporting 1 bit/s needs 1 Hz

- 1 GigE ➔ 1 CPU at 1 GHz
- 10 GigE ➔ 4 CPUs at 2.5 GHz



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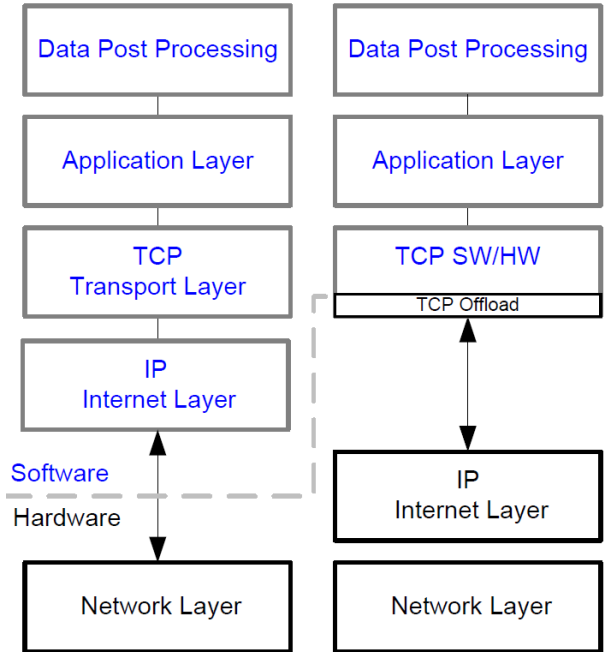
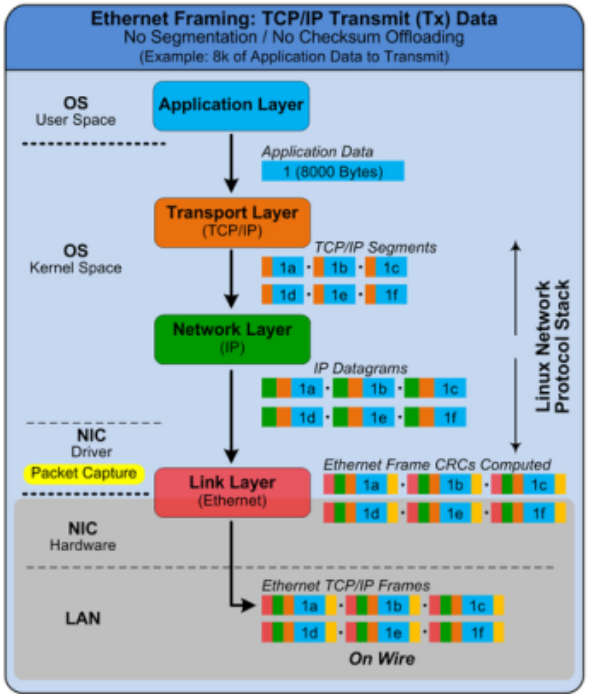
Better Bandwidth and Lower Latency via HW-Acceleration

- Smart algorithms to keep data local (in cache) and avoid uneccesary memory copies
  - Some datapath acceleration
  - Little control path acceleration
- State-of-the-art HW offloads the CPU
  - CRC computation
  - Segmenting

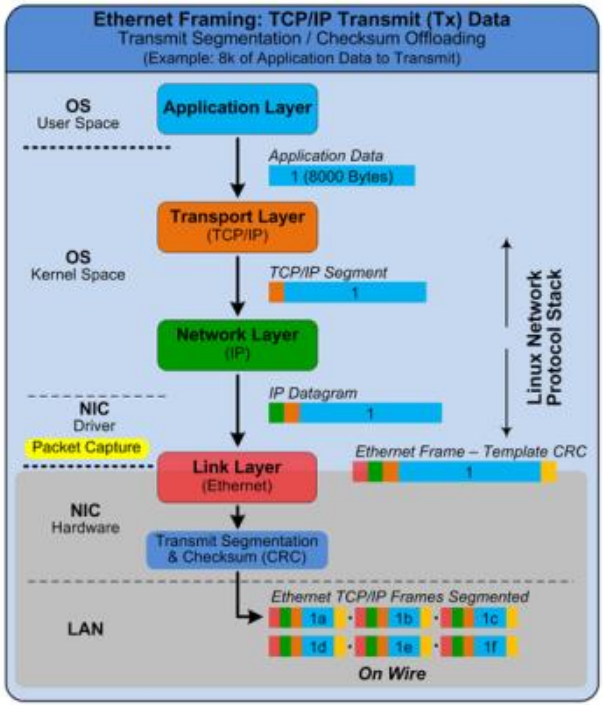


Example of State-of-the-Art Segmenting Offloading

- All software



- With HW acceleration



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Contributions from Fraunhofer HHI

Hardware Accelerated Internet Protocol

High Speed Hardware Architectures

2004
- Mask-less lithography systems
- Published in 2006
- XILINX VIRTEX-II

2008/09
- 1GbE TCP/IP stack
- Demonstrated at 2009 IFA
- Uncompressed full HD video transfer

IFA CONSUMER ELECTRONICS UNLIMITED The global innovations show.

2010
- 10GbE TCP/IP stack
- Uncompressed full HD video transfer
- Mask-less electron beam lithography

IFA CONSUMER ELECTRONICS UNLIMITED The global innovations show.

embedded world Exhibition&Conference ... it's a smarter world

2012
- 10GbE TCP/IP stack
- PCIe IP core
- Uncompressed full HD video transfer
- High Frequency Trading
- High Performance Computing
- Mask-less electron beam lithography

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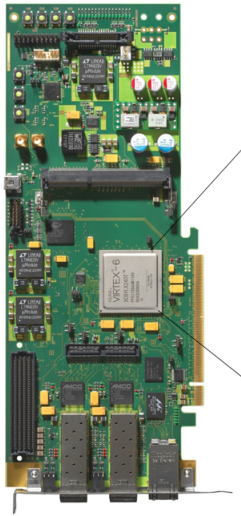
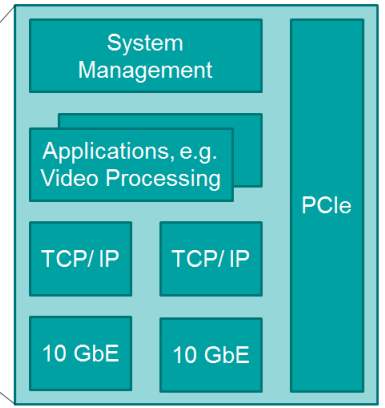
Hardware Accelerated Internet Protocol

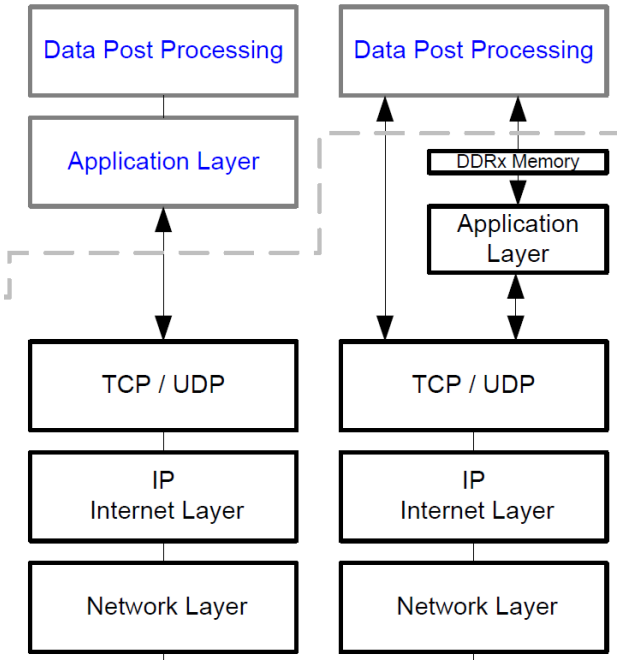
High Speed Hardware Architectures

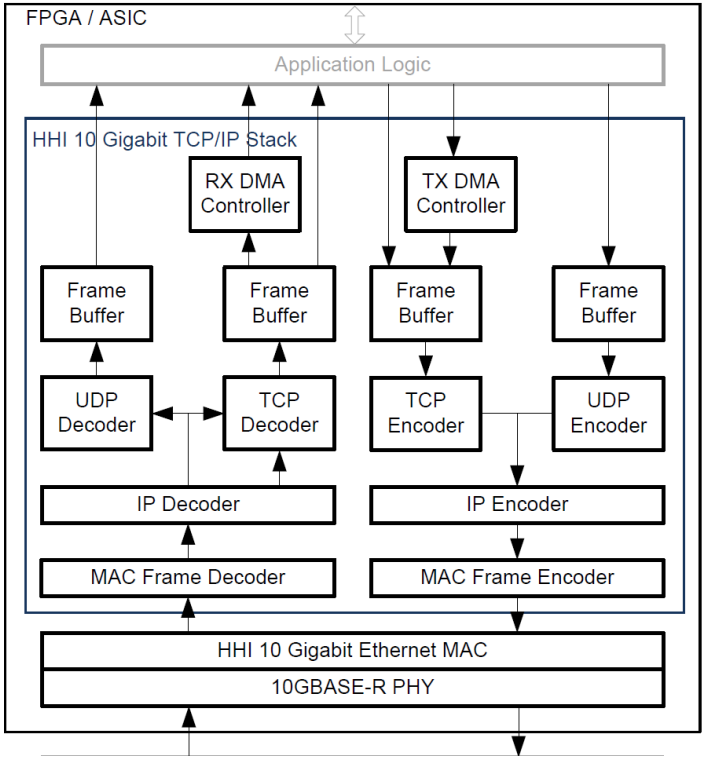




More Than TOE: FPGA-Based TCP/IP Processing

- Entire TCP / UDP protocol handling runs inside FPGA
- Option to run Application Layer processing in HW, too!





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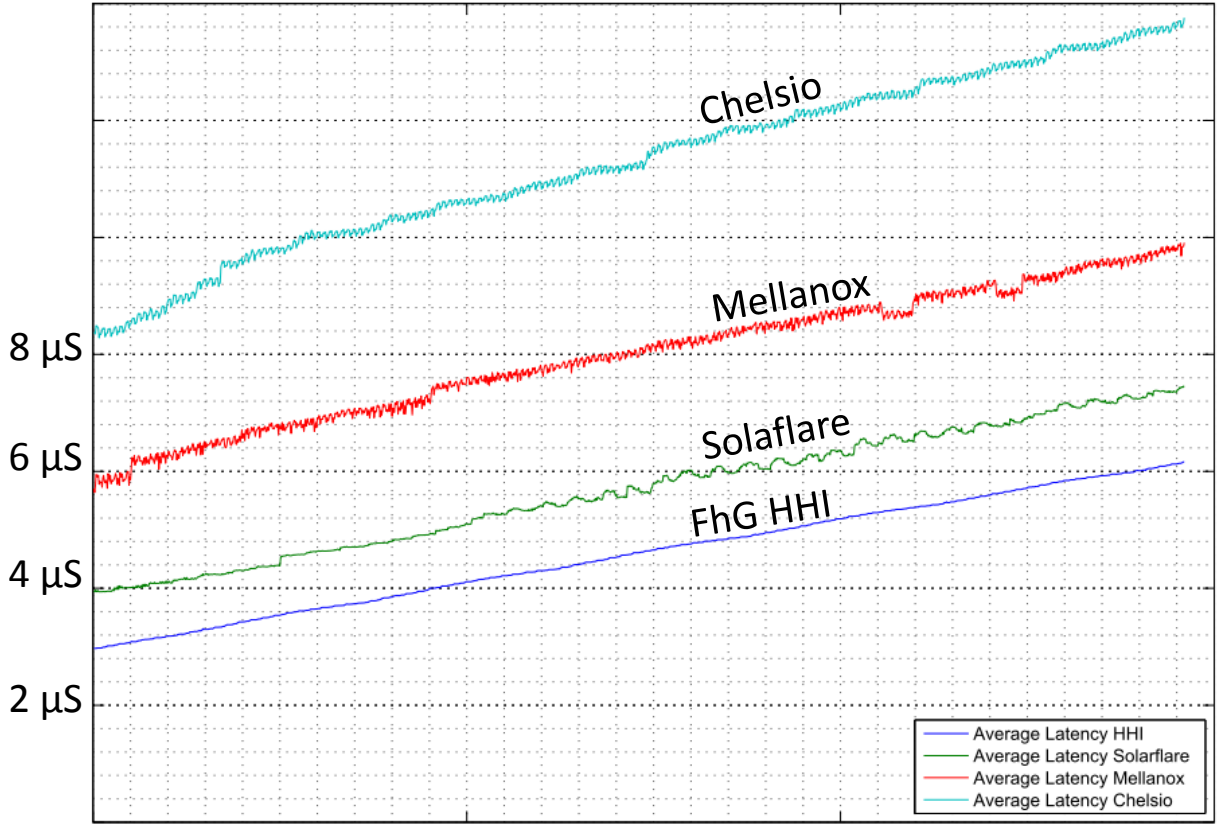
Average Latency Comparison

- Highly deterministic jitter measured in clock-cycles
- Scales with size of the segment
- Effectively offloads the CPU
- Delivers line-rate bandwidth over 10GigE



Contact Information

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