Langzeitverfügbarkeit mit All-Programmable System-on-Chips

- Dr. Endric Schubert, Missing Link Electronics

Backgrounder Endric Schubert

- 1991 Dipl.-Ing. ET, Univ. Karlsruhe
- 1996 Dr. rer. nat. Wilhelm-Schickard-Institut f. Informatik, Univ. Tübingen
- 1996 - 1998 Advanced Technology Group, Exemplar Logic / Mentor Graphics, EDA for FPGA & ASIC (RTL Synthesis)
- 1999 - 2003 CTO, Bridges2Silicon, Inc. (EDA, System-on-Chip Debug)
- 2003 – 2007 CTO, ESIC Solutions (Technology Advisory for EDA & Embedded Systems Design)
- Since 2003 Guest Lecturer at Institute for Microelectronics, Univ. of Ulm
- Since 2008 CTO, Missing Link Electronics (Design Services, Configurable Systems)
- 50+ Technical presentations, inventor on 20+ patents

Missing Link Electronics

- Founded 2008
- Silicon Valley HQ
- 12 Engineers in Neu-Ulm, GER

- Expertise
  - FPGA & Linux
  - I/O Connectivity, High-Speed SerDes
  - Acceleration of Algorithms & Protocols
  - Heterogeneous Multi-Core Processing

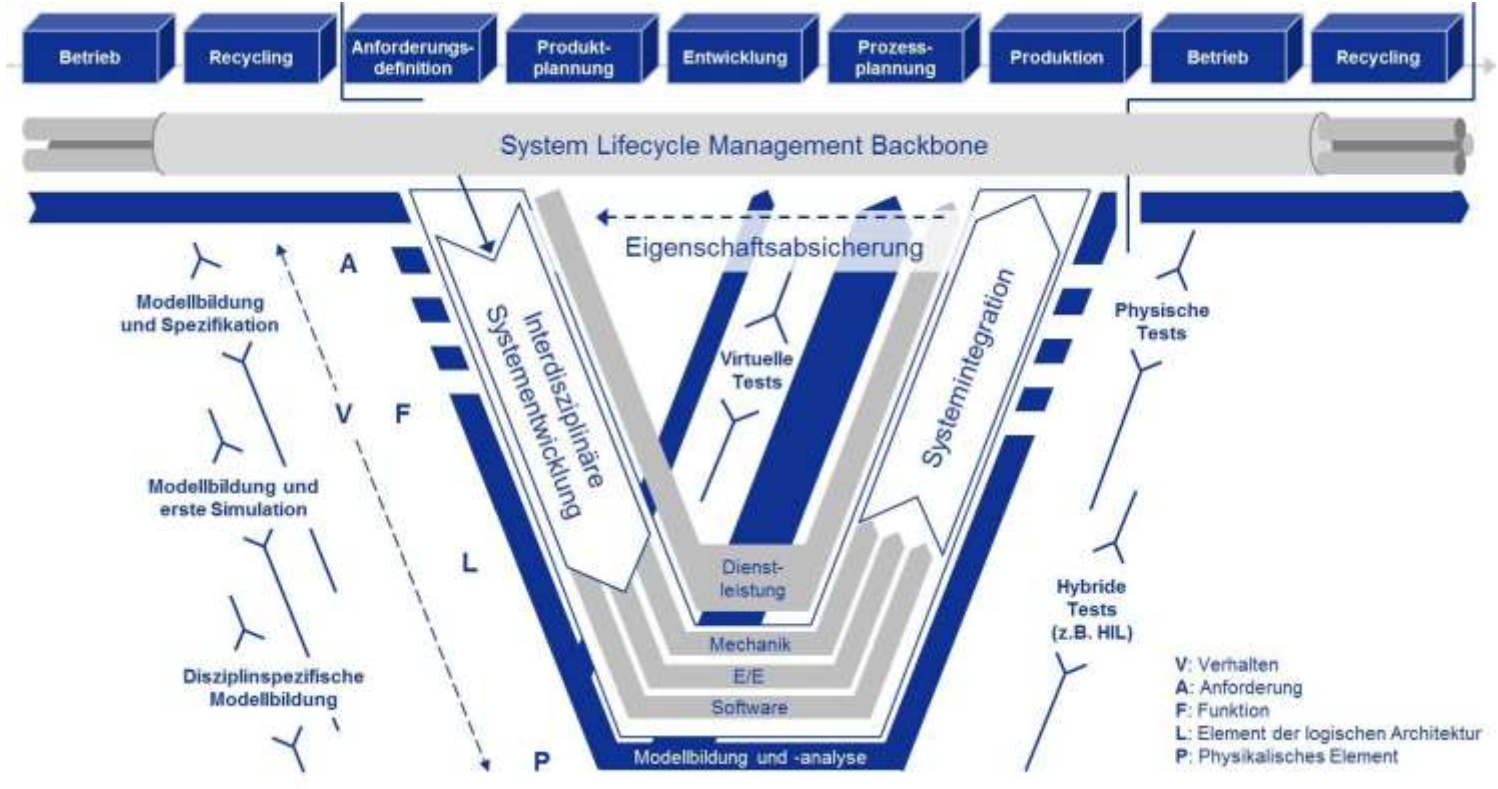
Bob Gardner
EDA

Endric Schubert
FPGA Technology

Sebastian Stiemke
Automotive / Industrial

Bob Barker
Semiconductors

Missing Link Electronics – Design Services



What We Really Do

Missing Link Electronics

- Technology Partners

IEEE Spectrum

SPECIAL REPORT: 50 YEARS OF MOORE'S LAW

The glorious history and inevitable decline of one of technology's greatest winning streaks

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Fifty years ago this month, Gordon Moore forecast a bright future for electronics. His ideas were later distilled into a single organizing principle—Moore's Law—that has driven technology forward at a staggering clip. We have all benefited from this miraculous development, which has forcefully shaped our modern world.

In this special report, we find that the end won't be sudden and apocalyptic but rather gradual and complicated. Moore's Law truly is the gift that keeps on giving—and surprising, as well.

The Multiple Lives of Moore's Law

Why Gordon Moore's grand prediction has endured for 50 years

30 Mar

The Death of Moore's Law Will Spur Innovation

As transistors stop shrinking, open-source hardware will have its day

31 Mar

Moore's Law Might Be Slowing Down, But Not Energy Efficiency

Miniaturization may be tough, but there's still room to drive down power consumption in modern computers

21 Mar

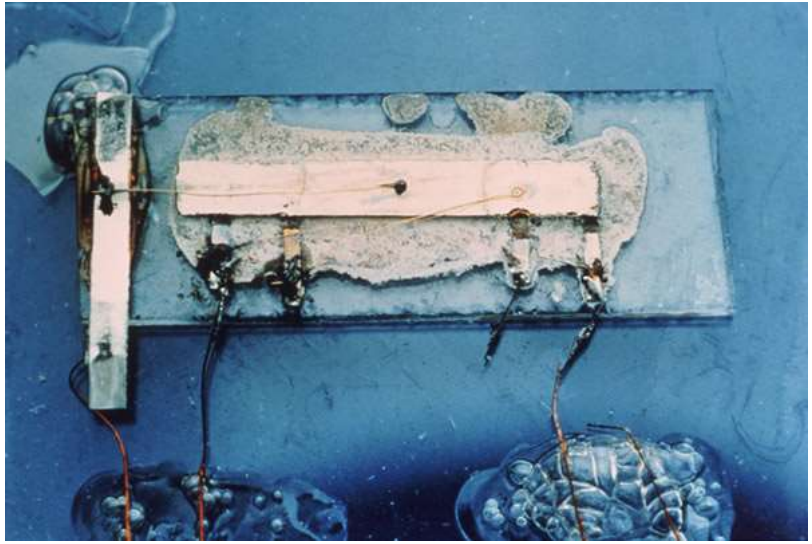
Gordon Moore: The Man Whose Name Means Progress

The visionary engineer reflects on 50 years of Moore's Law

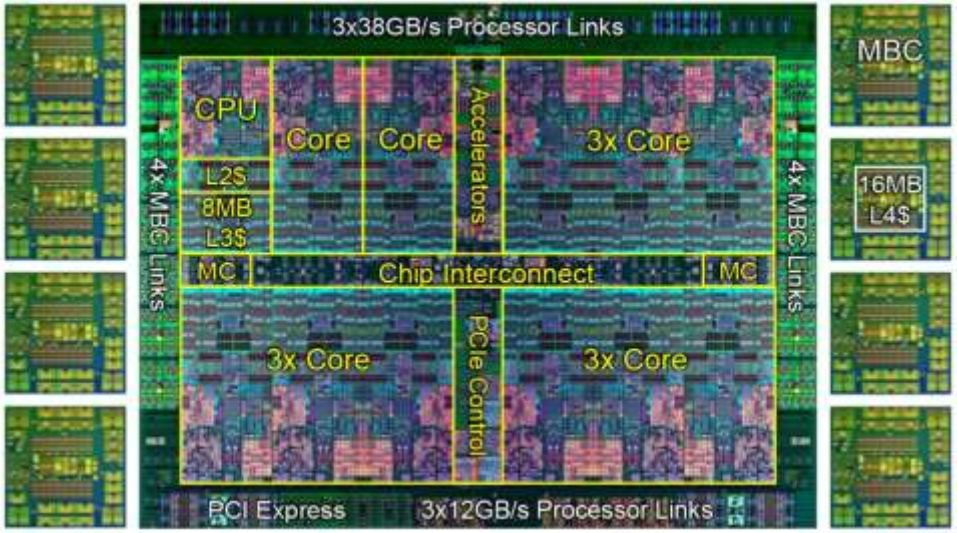
30 Mar

Moore’s Law in Two Pictures

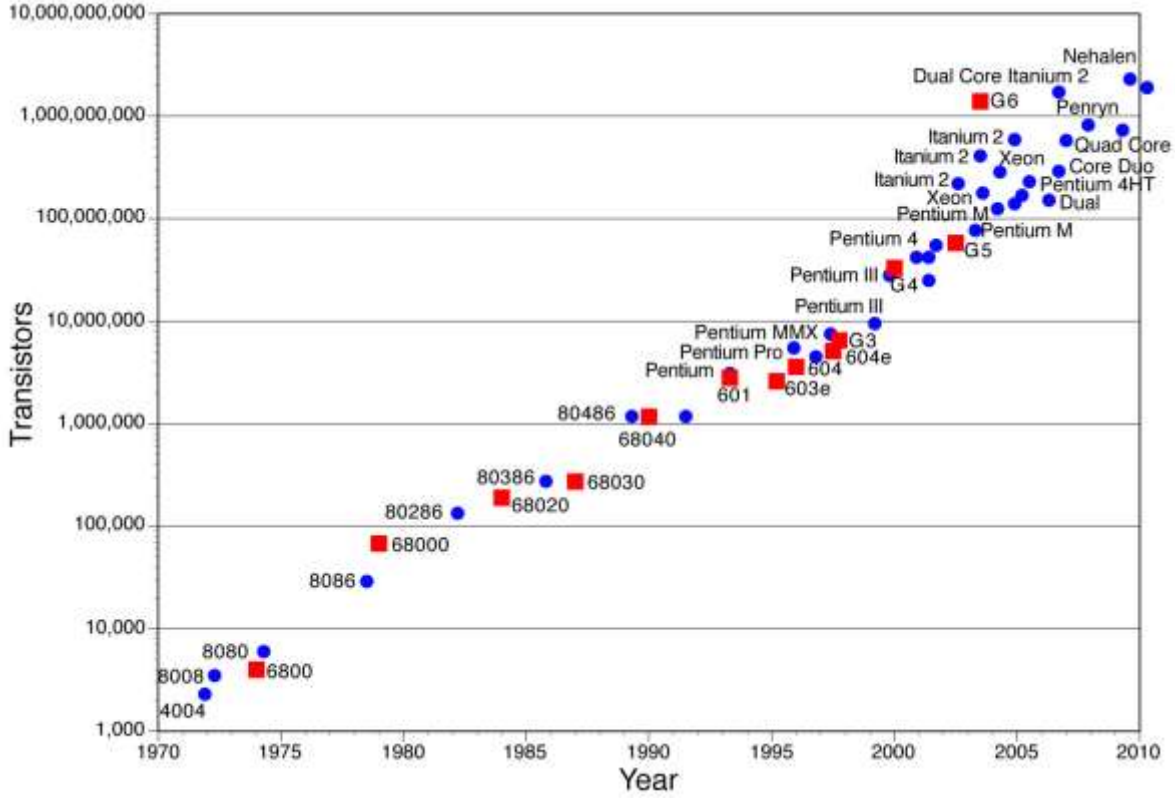
1958 IC - 1 Transistor
(Jack Kilby's first IC)



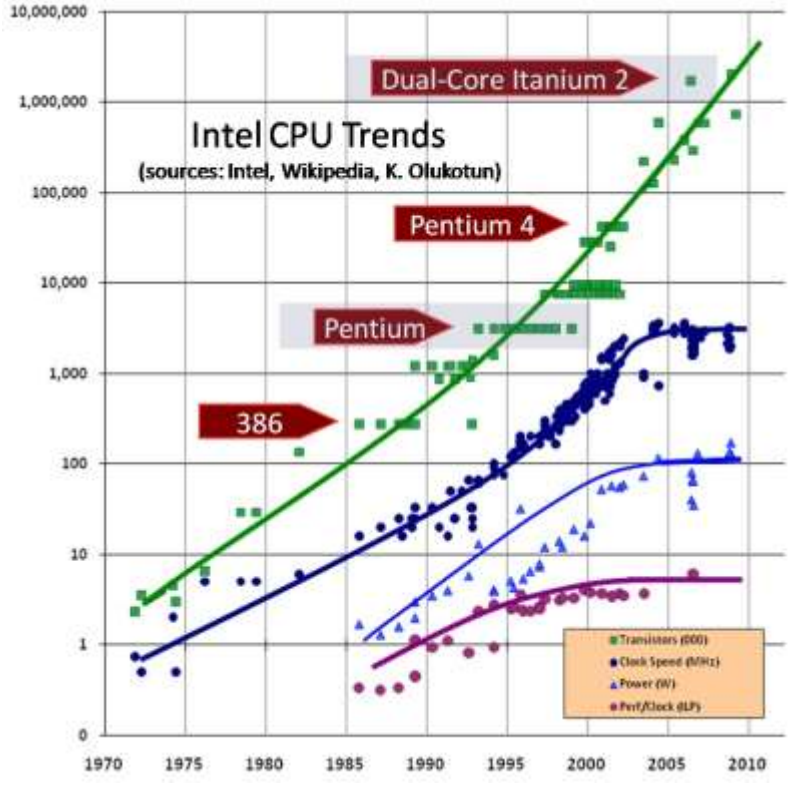
2015 IC – 4 billion transistors
(IBM Power8 CPU)



Moore‘s Law – 50 years and counting



Moore‘s Law – 50 years and counting … but



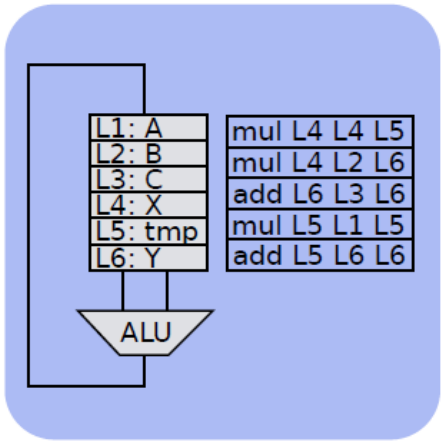
Hardware vs. Software Data Processing

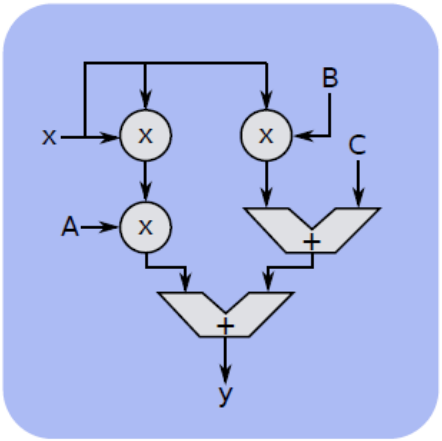
Sequential Processing with CPU

- C, C++ Program

Parallel Processing with Logic Gates

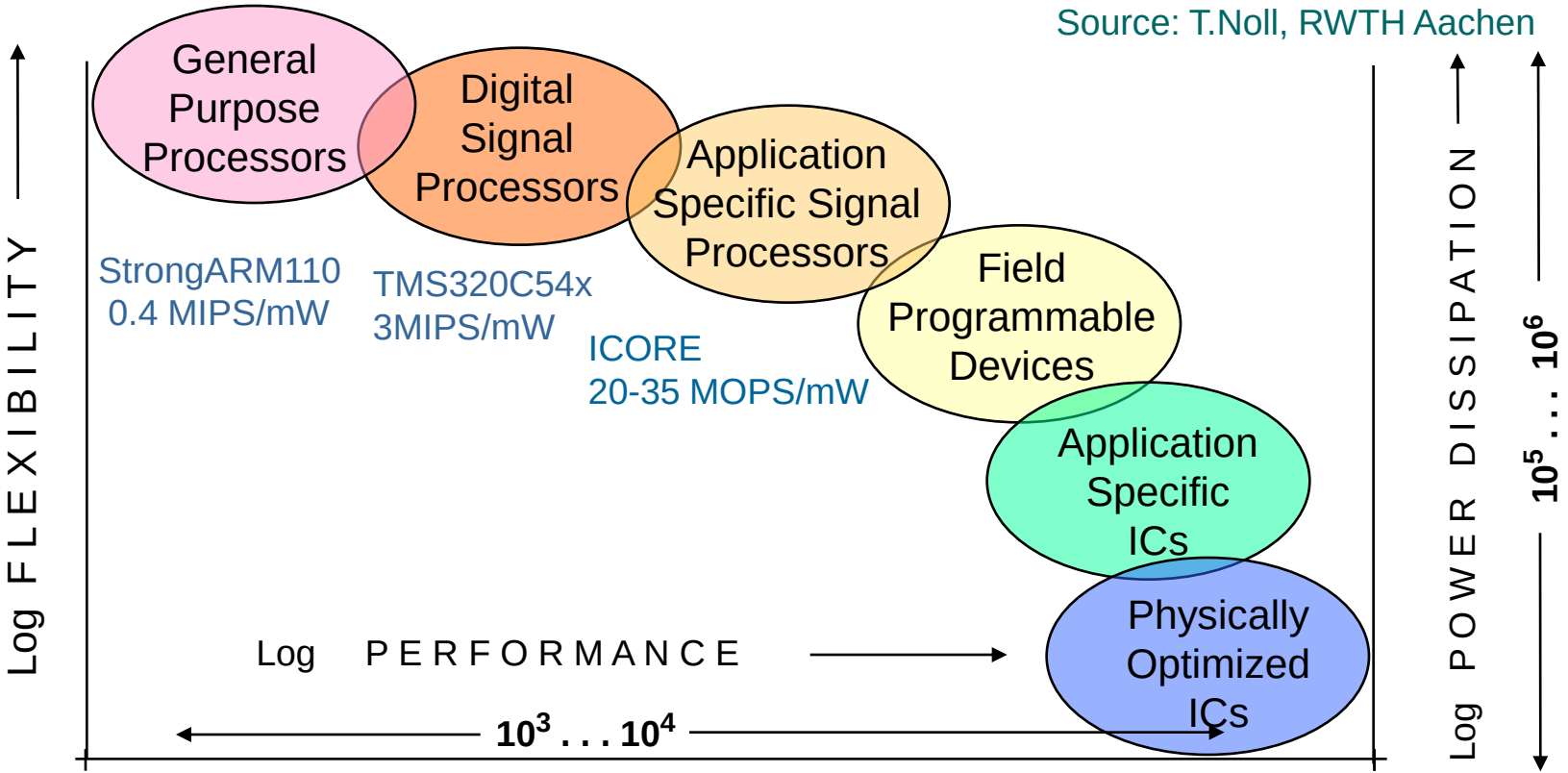
- VHDL, Verilog "Program"





Courtesy: Dr. Andre DeHon, UPenn

Choices for Implementing Embedded Systems

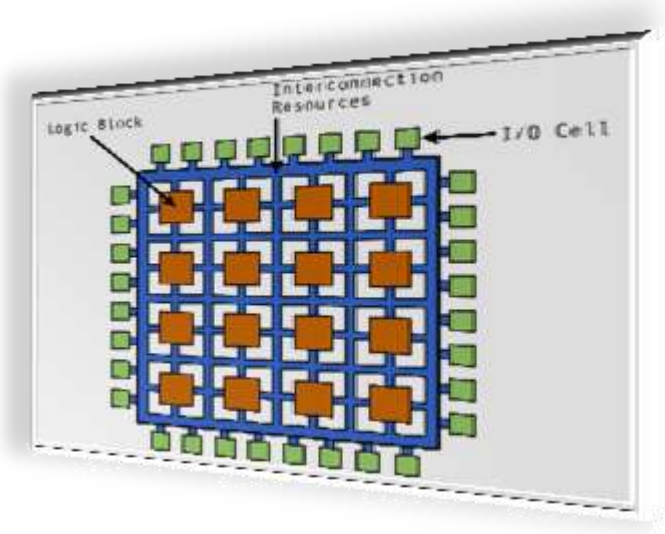


What is an FPGA (Programmable Logic)?

- A Field-Programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence " field-programmable" (Wikipedia)

- In their simplest form FPGAs contain:
  - Configurable Logic Blocks
    - AND, OR, Invert & many other logic functions
  - Configurable interconnect
    - Enabling Logic Blocks to be connected together
  - I/O Interfaces

- With these elements an arbitrary logic design may be created



FPGAs - Circa 1990

Common Use Cases:

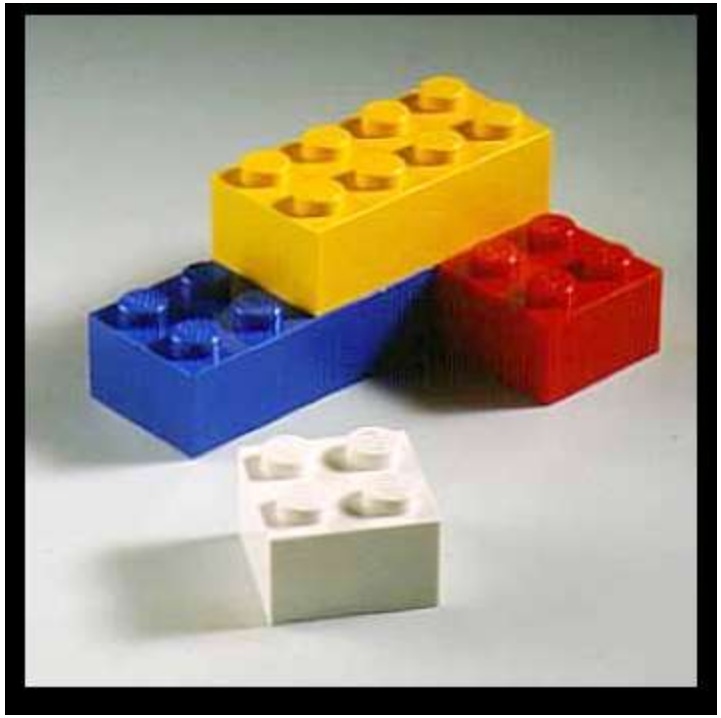
- Glue Logic
- Simple State Machines
- Prototyping

Pro: Easy to use

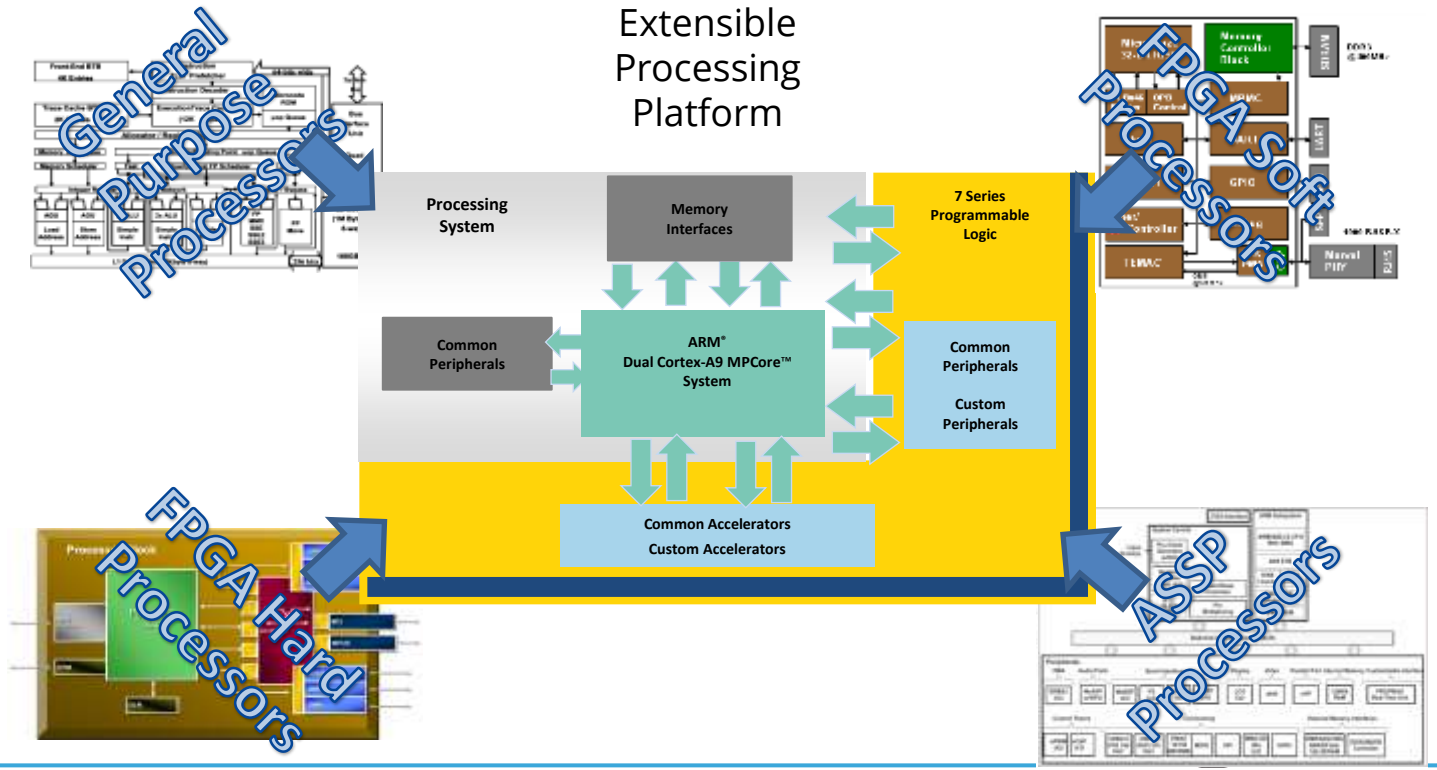
- Logic that could be connected Like LEGO blocks

Con: Resource limited

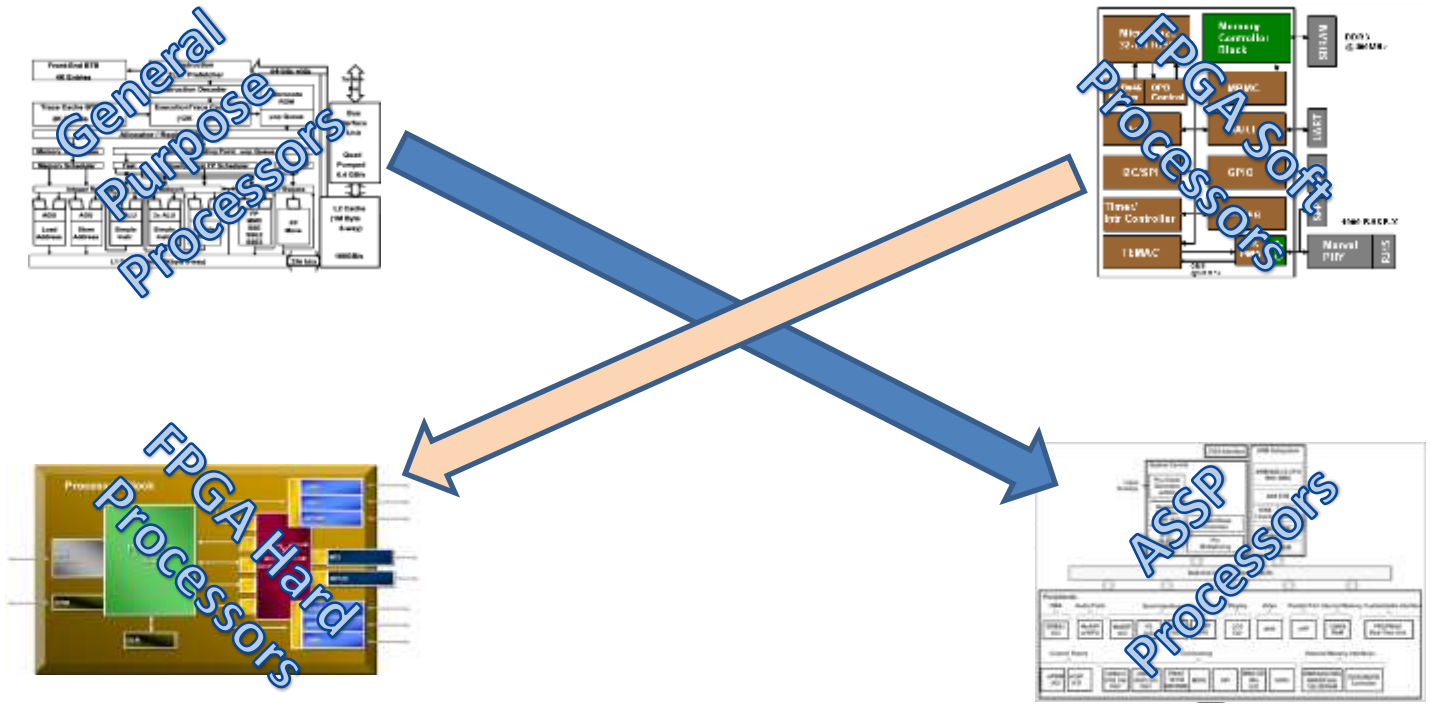
- Many FPGAs needed to implement one single CPU



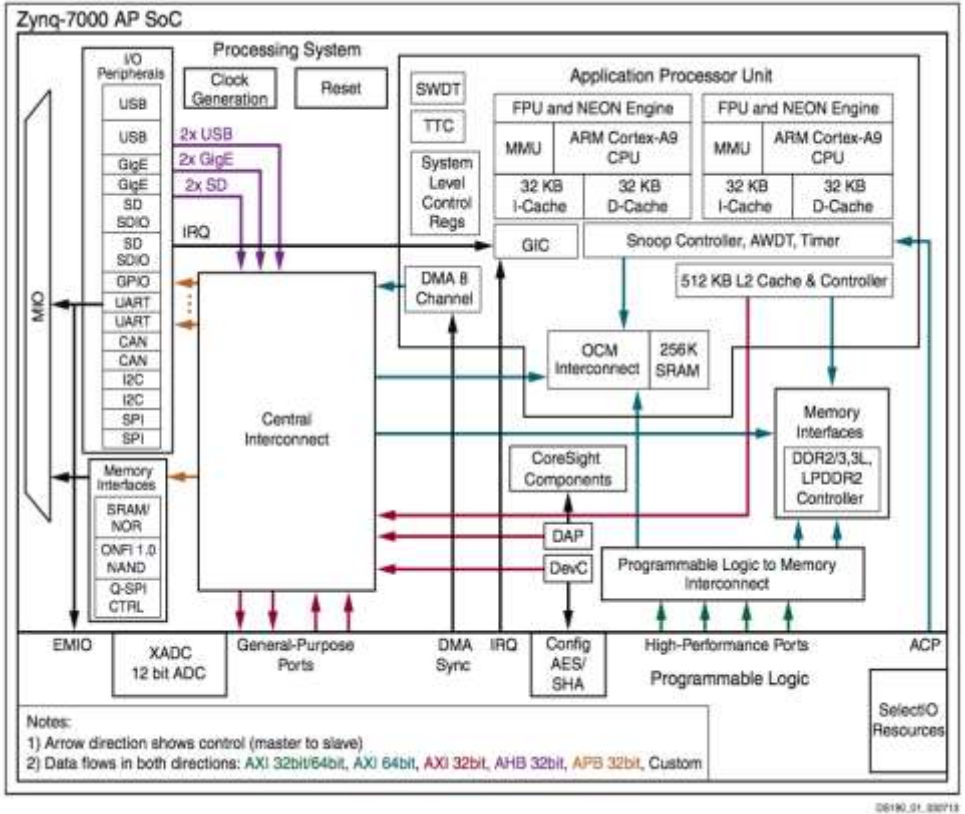
Convergence of Processing Systems

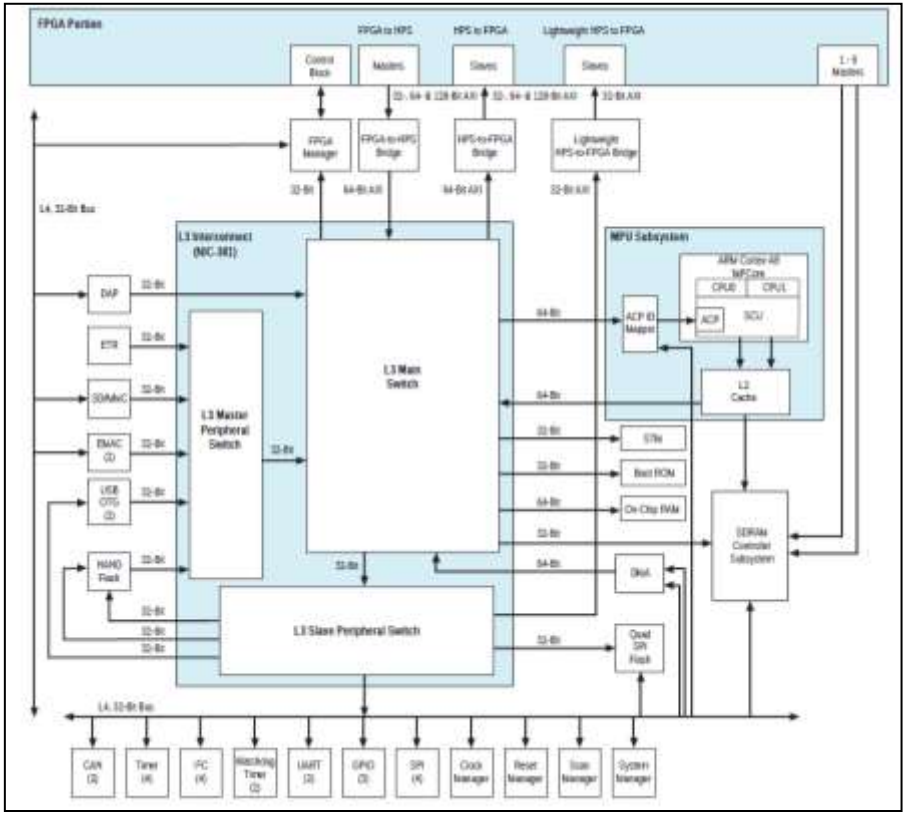


Convergence of Processing Systems



Multiple FPGA Vendors With Integrated CPUs





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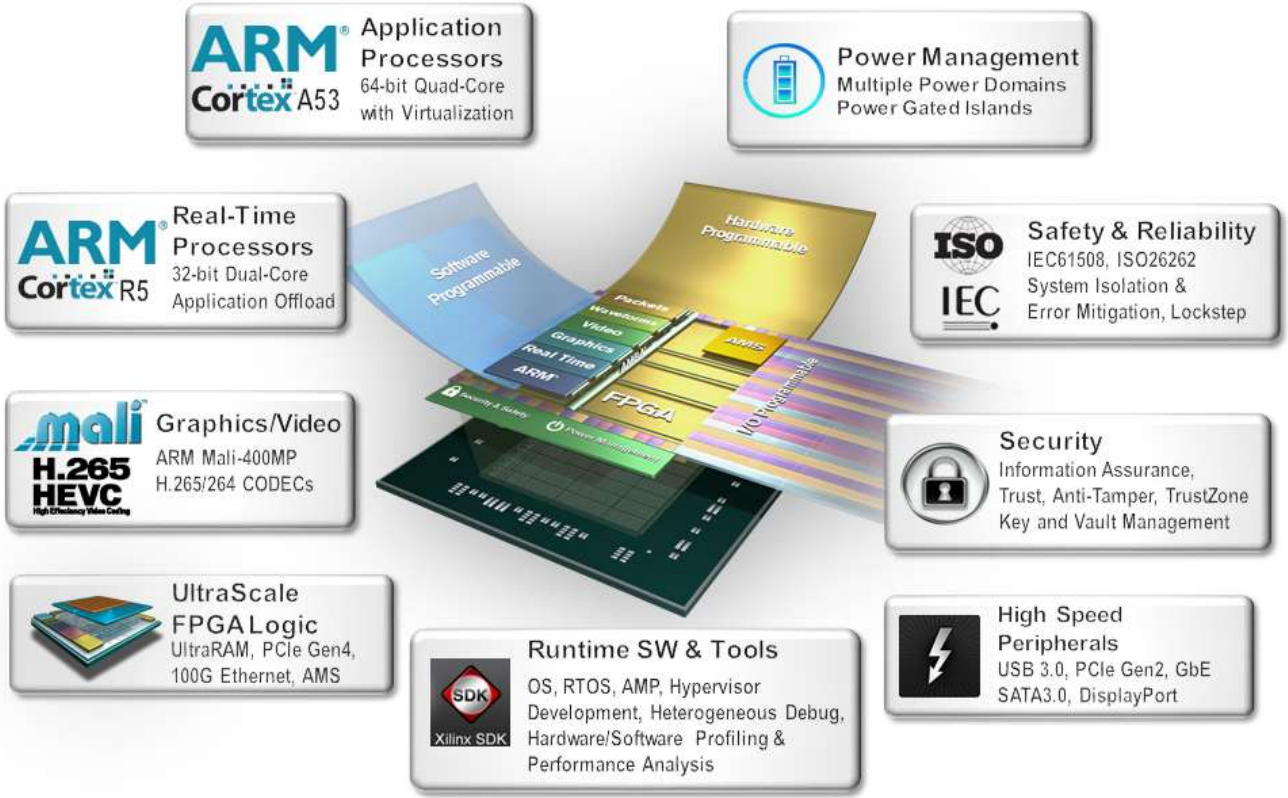
FPGA as All-Programmable Embedded System-on-Chip

- Programmable I/Os (LVTTL, LVDS, High-Speed SerDes)
- Programmable logic functions (State machines and dataflow)
- Programmable block interconnect (Buses and Network-on-Chip)
- Programmable Fixed-Function Processing (Ethernet MAC, Video Codecs)
- Programmable CPUs (for software processing with or w/o Operating Systems)



FPGA Vendors Fully Support Embedded and Safety

Building Smarter Factories With Smarter Devices

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Xilinx Safety Solution – Certified by TÜV

IEC 61508

A Safety system is Functionally Safe if systematic, random and common cause failures do not lead to malfuction

Random and Common Cause Failures
Quantitative assessment

- Industry Lowest SEU Fit rates
  - SEU mitigation IP
  - FIT Rate calculator
    - Essential and Critical Bit analysis
- Isolation Design Flow and Isolation Verification Flow
- Common Cause Failure Mitigation
- Power Analysis tools
- Xilinx and supply chain committed to Quality and Quality management
  - ISO9000/QML/TL9000/TS16494

Systematic Failures
Qualitative assessment

- Qualified tools - ISE 14.2 , 14.7
- Safety Manual, Certificate and test report
- Isolation Design Flow and Isolation Verification Tools

IEC 61508	SIL1 to SIL3
ISO 26262	ASIL A to ASIL D

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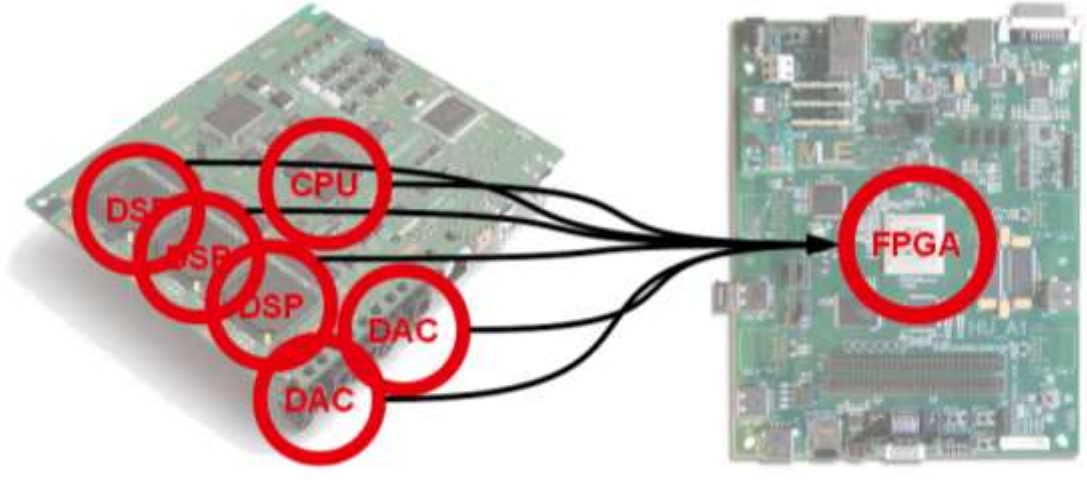
FPGA: Software-Defined Printed Circuit Boards

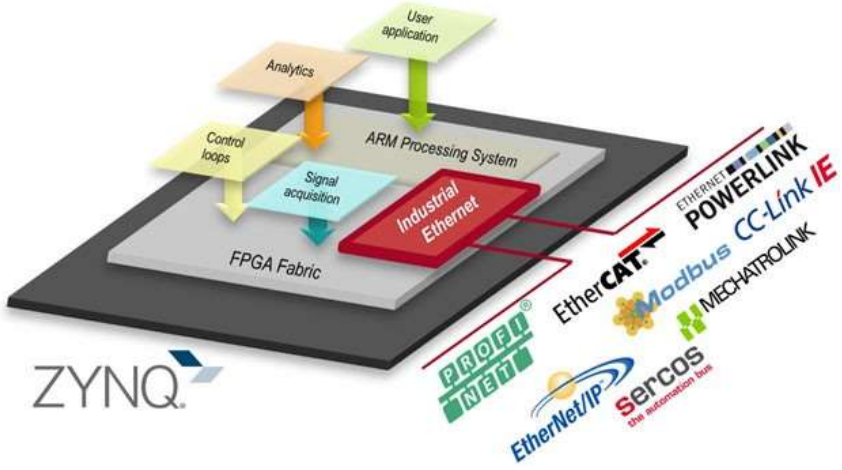


Integrating individual microcontroller, DSP, ADC/DAC and I/O controller devices into one single FPGA-based System-on-a-Chip gives more flexibility for hardware changes without re-spinning a new PCB.

Programmable Connectivity

Different I/O Standards & Protocols

- Single-ended LVTTL
- Differential LVDS
- High-Speed SerDes Transceivers
- Multi-Protocol
  - SPI, IIC, MMC, …
  - CAN, LIN, FlexRay, …
  - PCIe Gen1, Gen 2, Gen 3, Gen 4
  - SATA-6G, SAS-12G, UFS-12G, …
  - USB, Ethernet, …
- Analog I/O via hard blocks or
  Soft Analog Sigma-Delta Modulators



FPGA Performance Chart

Data from http://www.xilinx.com/products/silicon-devices/fpga.html

FPGA Comparison Table

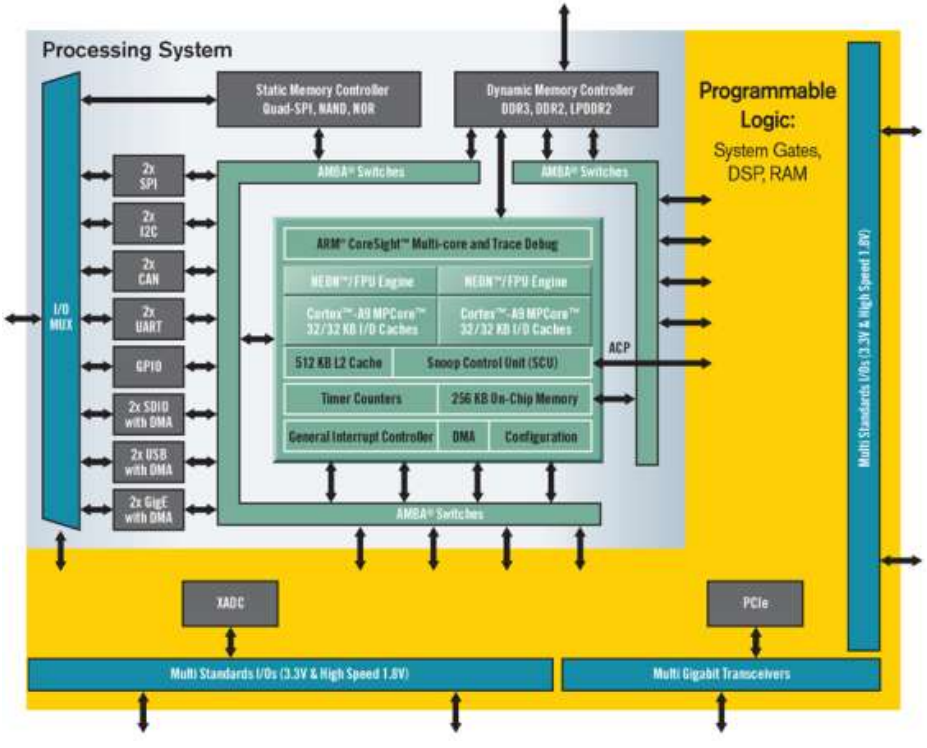
	Kintex-7	Virtex-7	Kintex UltraScale	Kintex UltraScale+	Virtex UltraScale	Virtex UltraScale+
Logic Cells (K)	478	1,955	1,161	915	4,433	2,863
UltraRAM (Mb)	-	-	-	36.0	-	432.0
Block RAM (Mb)	34	68	76	34.5	132.9	94.5
DSP Slices	1,920	3,600	5,520	3,528	2,880	11,904
DSP Performance (symmetric FIR)	2,845 GMACs	5,335 GMACs	8,180 GMACs	6,287 GMACs	4,268 GMACs	21,213 GMACs
Transceiver Count	32	96	64	76	120	128
Maximum Transceiver Speed (Gb/s)	12.5	28.05	16.3	32.75	30.5	32.75
Total Transceiver Bandwidth (full duplex) (Gb/s)	800	2,784	2,086	2,478	5,886	8,384
Memory Interface (DDR3)	1,866	1,866	2,133	2,133	2,133	2,133
Memory Interface (DDR4)	-	-	2,400	2,667	2,400	2,667
PCI Express®	x8 Gen2	x8 Gen3	x8 Gen3	x8 Gen 4 x16 Gen 3	x8 Gen3	x8 Gen 4 x16 Gen 3

Power vs. Performance of All-Programmable SoCs

SoC FPGA as (yet) another computer

	Intel i7-4770	Xilinx Zynq 7045
Compute	~100 GFLOPS	5 GFLOPS (PS) 778 GFLOPS (PL)
TDP	84 W	<20 W (typ)

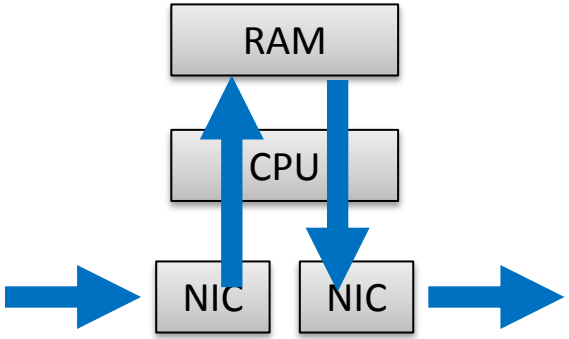
SOC FPGA has 4x more compute
With ¼ the power dissipation!



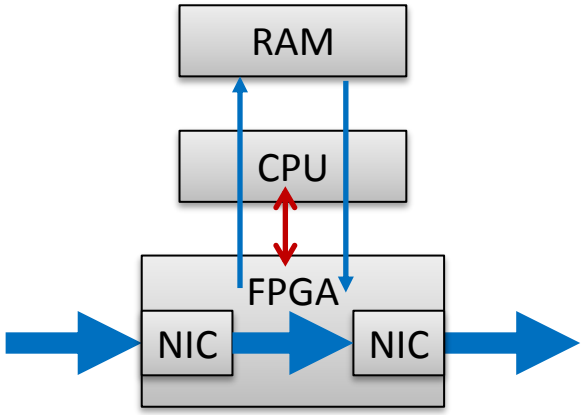
[http://www.xilinx.com/products/technology/dsp.html]

Predictable Architectures For Higher Performance

Current architecture limits maximum performance to total DMA bandwidth.

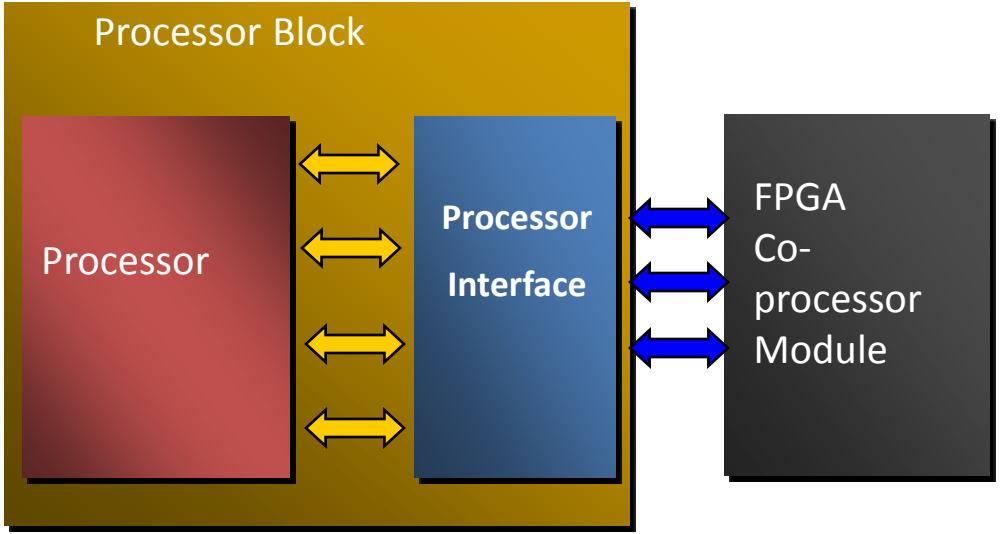


Separate control flow and dataflow for higher bandwidth via FPGA-based inline processing, integrates NIC into FPGA fabric.



Coprocessors Enable Acceleration of Your Software

- Direct connection between processor and a soft coprocessor

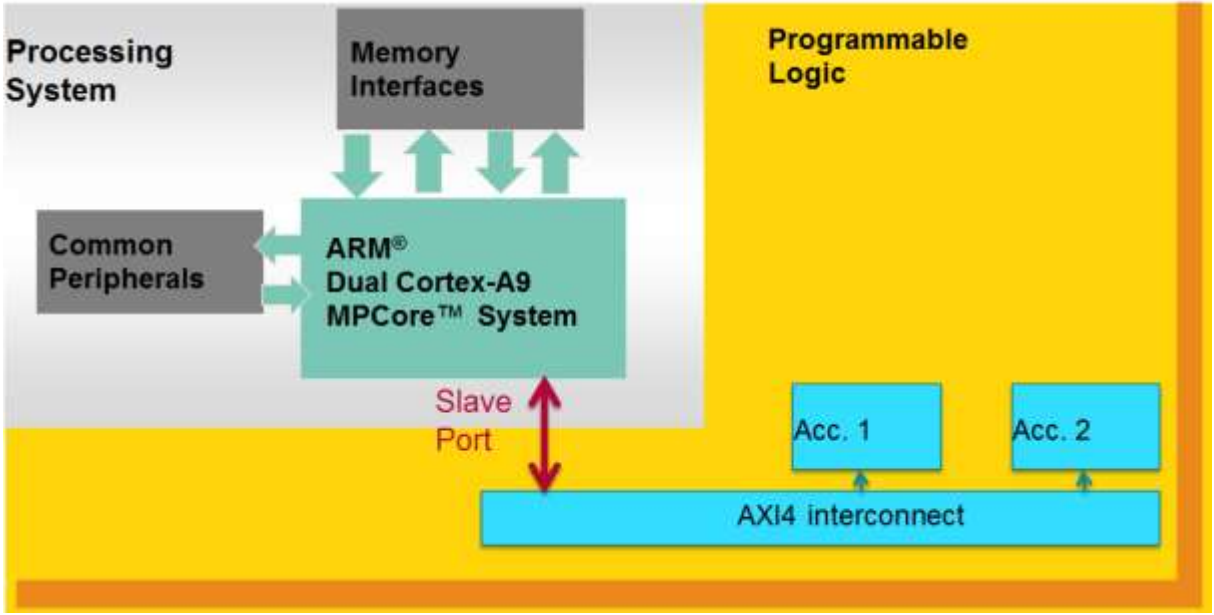


- Provides offloading of processing task
- Enables Dramatic Performance Improvements

Application	Acceleration
Back Projection (FP)	8 x
4096 Point FFT	6 x
Matrix Multiply (FP)	20 x

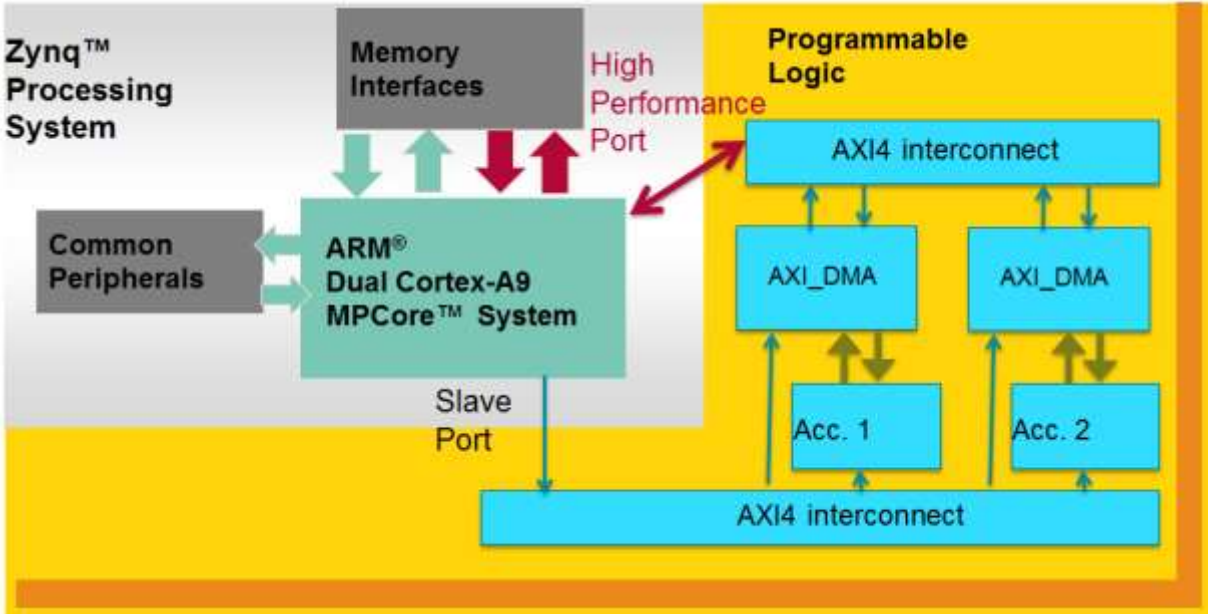
Accelerator Options: Attached as Slave

- Pro: Simple System Architecture, Simple Register Interface
- Con: Limited communication bandwidth



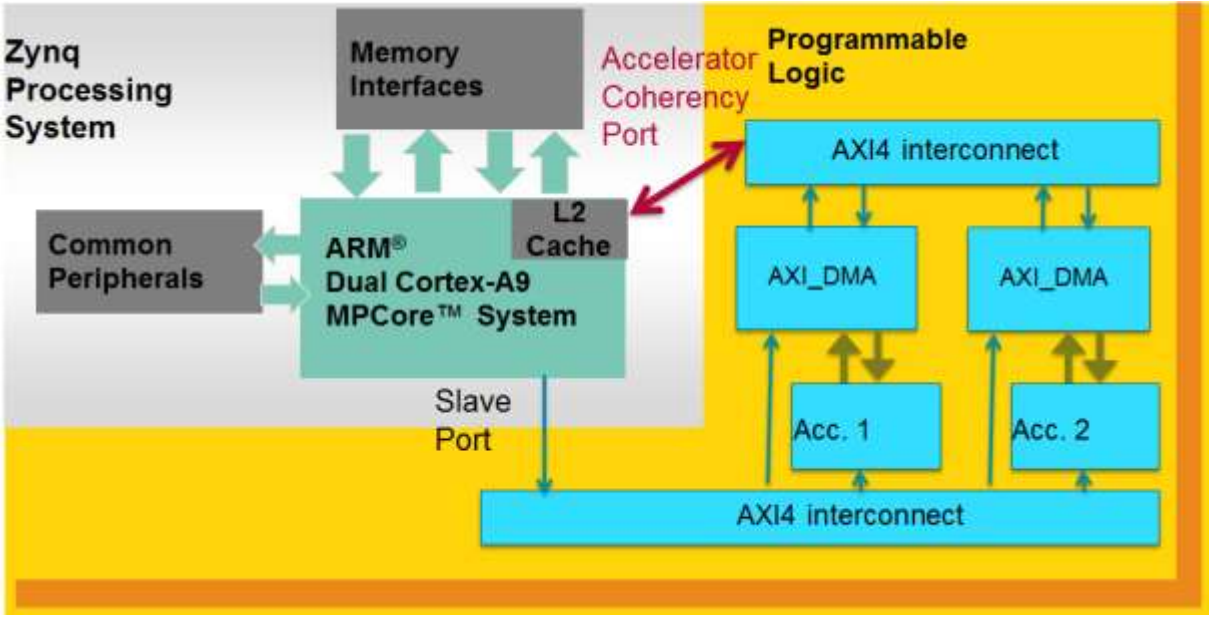
Accelerator Option: Attached as a Master (High Performance Port to Memory)

- Pro: High Data Bandwidth
- Con: Increased Design Complexity, Increased Latency



Accelerator Option: Attached as a Master (Coherent DMA to Level-2 Cache)

- Pro: Low latency, high data bandwidth for short bursts
- Con: Increased design complexity, adverse caching effects on SW



Accelerator Option: ARM Built-in NEON Engine

- 4096 point FFT – Complex 32 bit floating point
  - ARM processor alone – 830 usec
  - NEON SIMD engine – 571 usec
  - Hardware in PL fabric – 129 usec

45% FFT Acceleration Using NEON Instructions and ARM NE10 DSP Library

6.4x FFT Acceleration Using ACP Attached Accelerator

FPGAs Today (2015)

Common Use Cases:

- Complete Embedded Processing in Integrated Systems-on-Chip
- High-Performance Computing, DSP, Terabit Packet processing

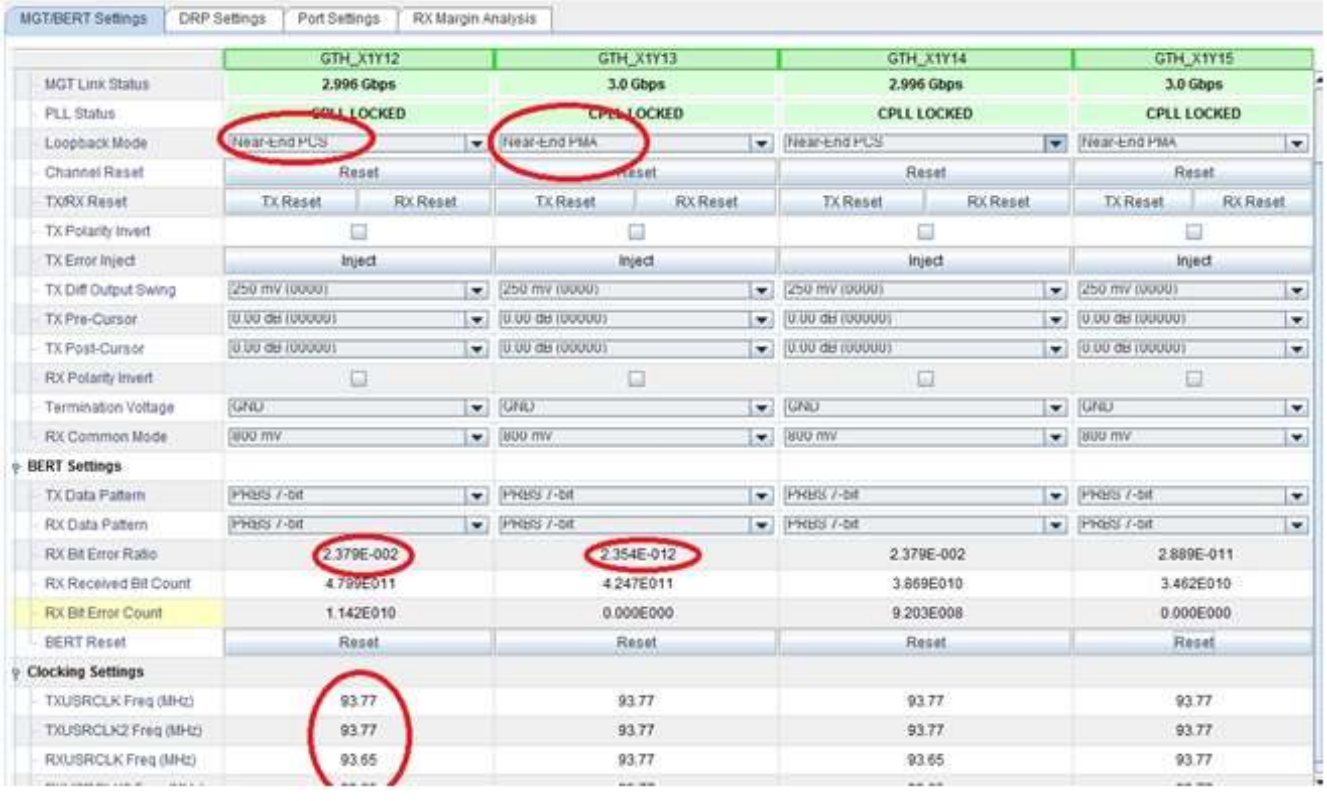
Pro: Lots of resources

- Many CPUs fit into one single FPGA

Con: Expert programming skills needed

- I/O standards & protocols in High-Speed SerDes, HW-SW-Interfaces for parallel processing

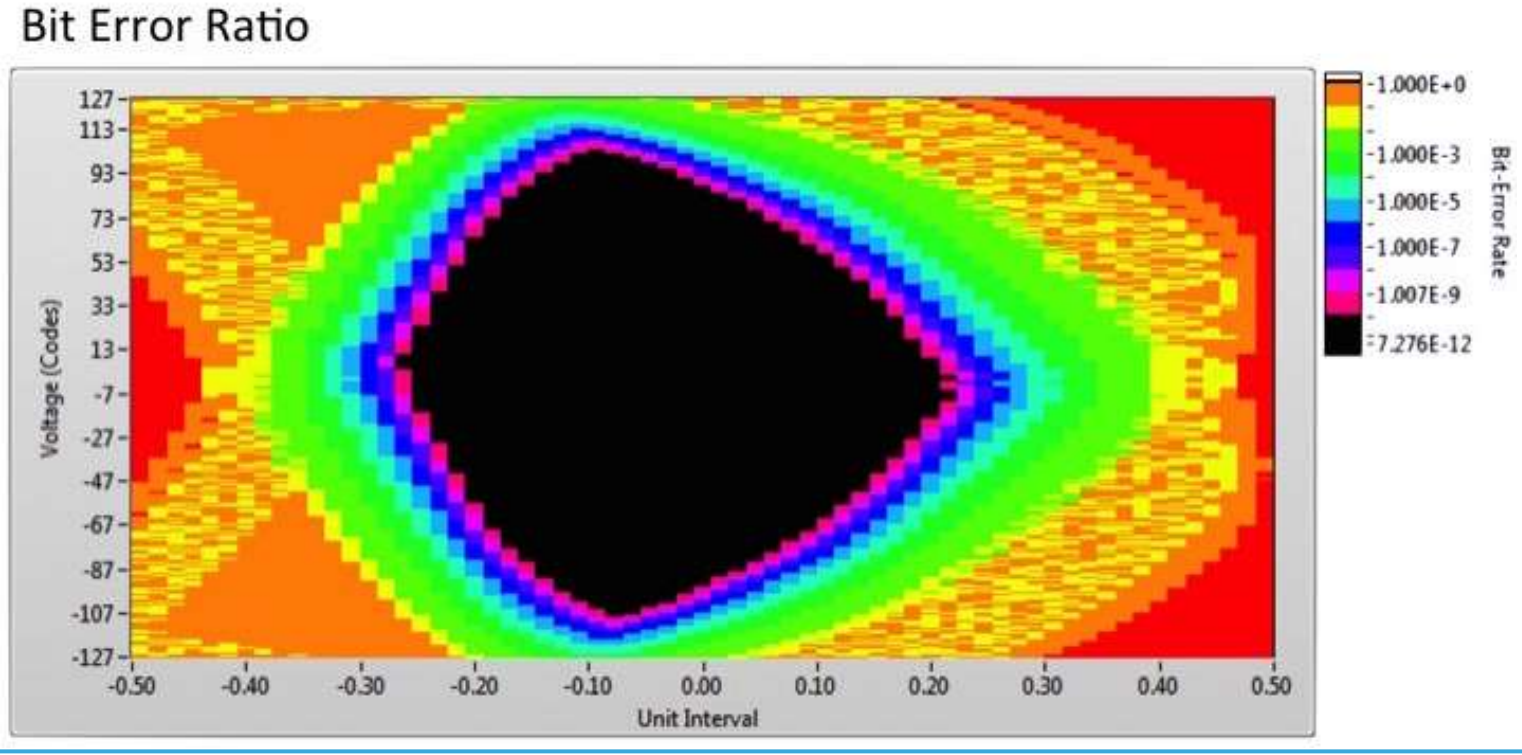
Design and Verification for FPGAs - I/O Programming



MGT/BERT Settings | DRP Settings | Port Settings | RX Margin Analysis

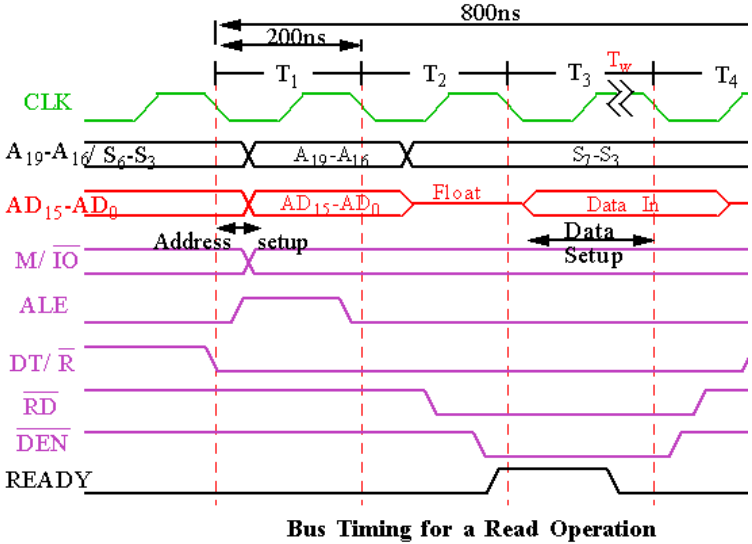
	GTH_X1Y12	GTH_X1Y13	GTH_X1Y14	GTH_X1Y15
MGT Link Status	2.996 Gbps	3.0 Gbps	2.996 Gbps	3.0 Gbps
PLL Status	CPLL LOCKED	CPLL LOCKED	CPLL LOCKED	CPLL LOCKED
Loopback Mode	Near-End PCS	Near-End PMA	Near-End PCS	Near-End PMA
Channel Reset	Reset	Reset	Reset	Reset
TX/RX Reset	TX Reset / RX Reset	TX Reset / RX Reset	TX Reset / RX Reset	TX Reset / RX Reset
TX Polarity Invert	☐	☐	☐	☐
TX Error Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	250 mV (0000)	250 mV (0000)	250 mV (0000)	250 mV (0000)
TX Pre-Cursor	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)
TX Post-Cursor	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)
RX Polarity Invert	☐	☐	☐	☐
Termination Voltage	GND	GND	GND	GND
RX Common Mode	800 mV	800 mV	800 mV	800 mV
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	2.379E-002	2.354E-012	2.379E-002	2.889E-011
RX Received Bit Count	4.799E011	4.247E011	3.869E010	3.462E010
RX Bit Error Count	1.142E010	0.000E000	9.203E008	0.000E000
BERT Reset	Reset	Reset	Reset	Reset
Clocking Settings				
TXUSRCLK Freq (MHz)	93.77	93.77	93.77	93.77
TXUSRCLK2 Freq (MHz)	93.77	93.77	93.77	93.77
RXUSRCLK Freq (MHz)	93.65	93.77	93.65	93.77

Design and Verification for FPGAs - I/O Verification



Design and Verification for FPGAs – Digital Logic Design

- Typically Hardware Description Languages (HDL) are used such as Verilog and VHDL.
- Designer must describe all 4 dimensions: functionality, structure, parallelism, timing



Bus Timing for a Read Operation

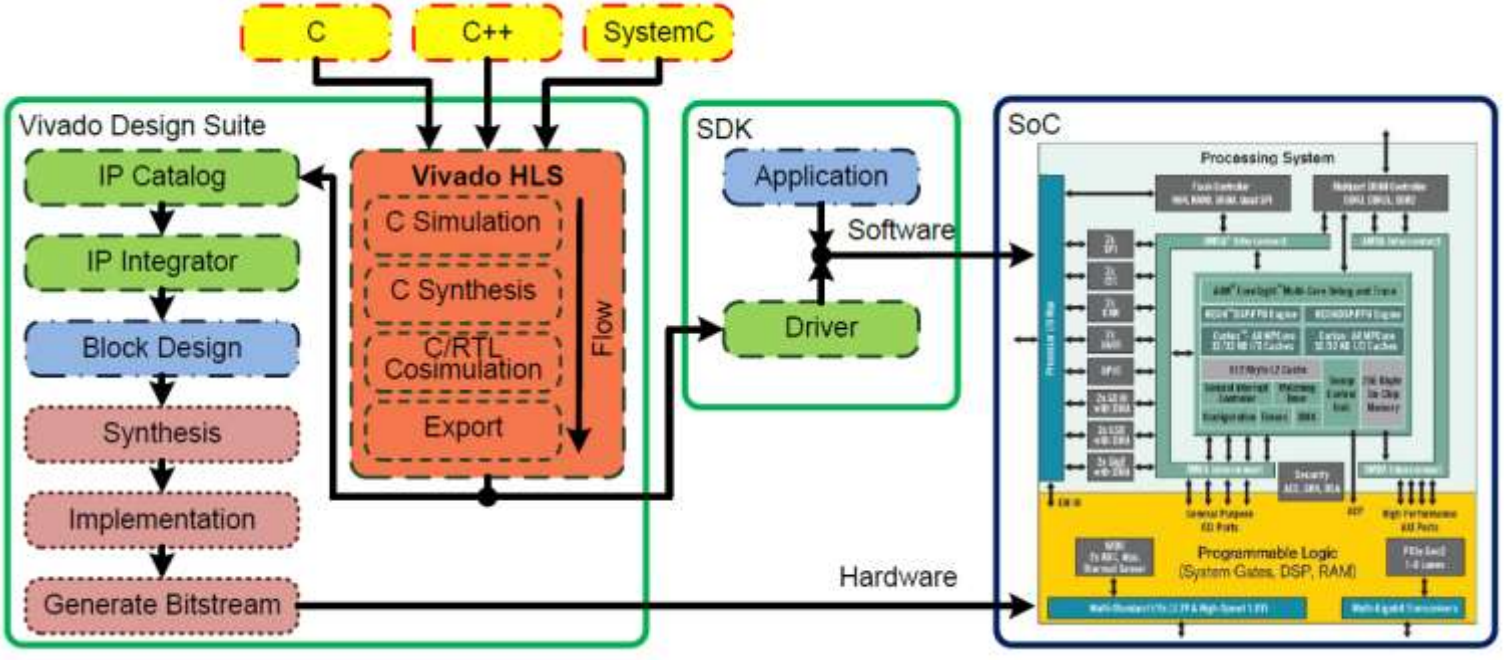
```
ENTITY counter IS
  PORT(count_val: OUT integer;
  clk: INOUT BOOLEAN);
END ENTITY counter;

ARCHITECTURE proc OF counter IS
  SIGNAL cnt: integer;
BEGIN
  p: PROCESS
  BEGIN
    WAIT ON clk´event and clk=´1´;
    cnt <= cnt+1;
  END PROCESS p;

  count_val <= cnt;
END ARCHITECTURE proc;
```

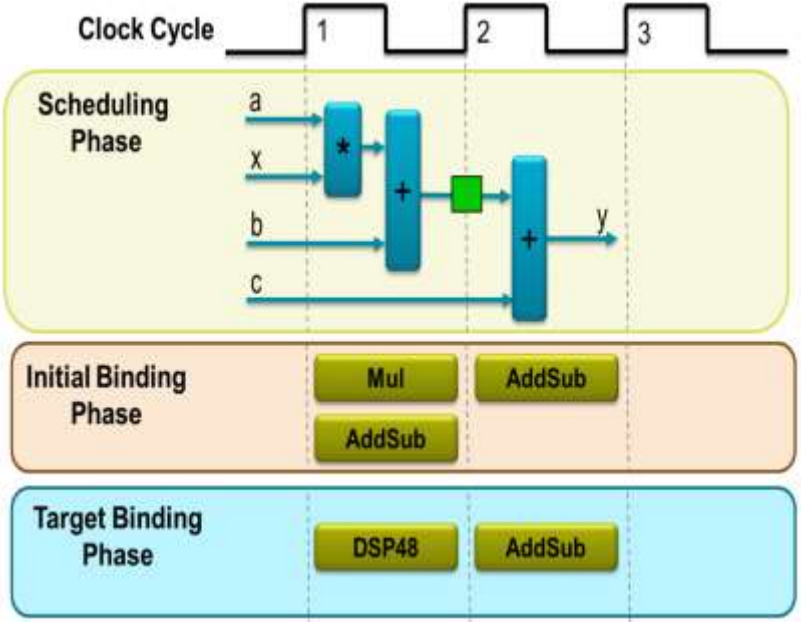
High-Level Synthesis Design Flow for SoC FPGA

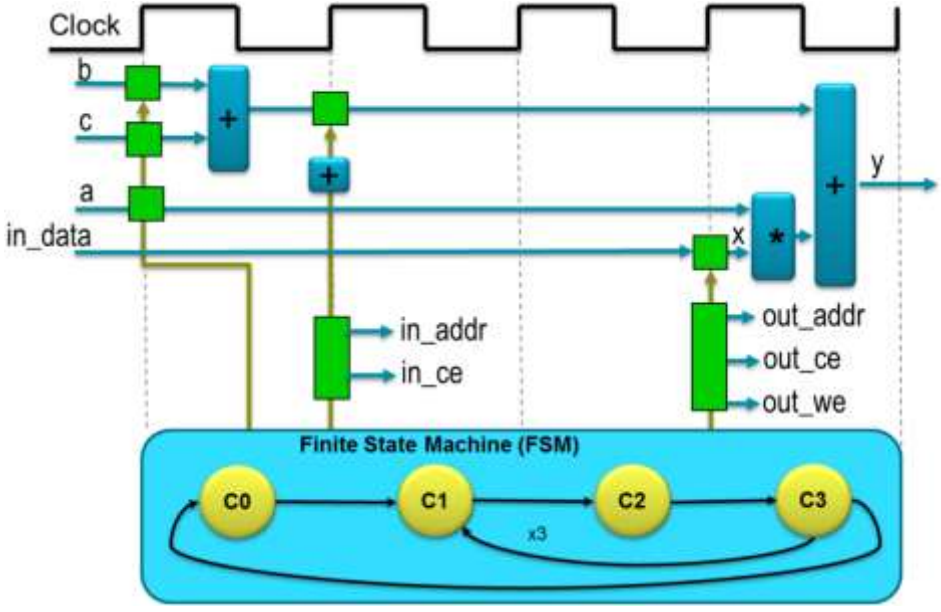
- Input C/C++/SystemC into High-Level Synthesis to generate VHDL/Verilog code



Working Principles of High-Level Synthesis

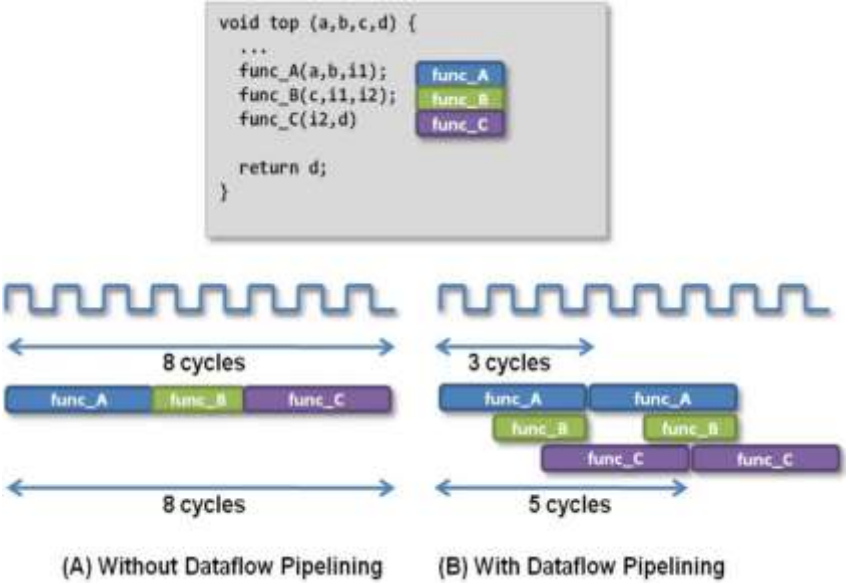
- Design automation runs scheduling and resource allocation to generate RTL code comprising data path plus state machines for control.



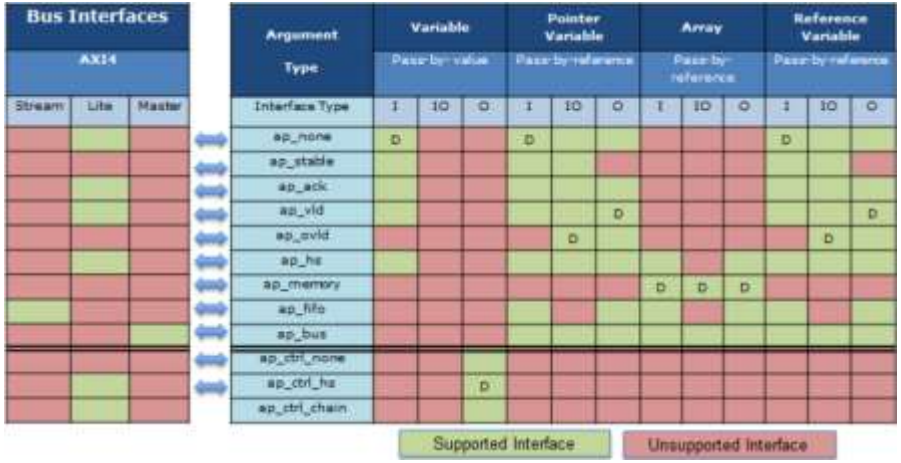


Benefits of High-Level Synthesis

- Automatic performance optimization via parallelization at dataflow level



- Automatic interface synthesis and code generation for variety of real-life HW/SW connectivity



Modern FPGAs Enable On-Chip-Debug and Verification

- FPGA is not the DUT!
- FPGA can be the DUT
  plus the TestBench
  plus extra on-chip debug

- With on-chip logic analyzers, or on-chip custom debug circuitry, you can analyze and fix your DUT without messy extra hardware setups!

Agile Design and Verification for Modern FPGAs

Abstraction Layer	Example	Design	Verification
Board Level	PCB, chipsets, interfaces, media, etc.	PCB, System Design	Rapid Prototyping In System Debugging
Electronic System Level (ESL)	System-on-Chip	GUI, memeory map, buses, NetworkOnChip	System C models, Bus Functional Models
Functional Blocks	H.264, FEC, AES	In-house or 3rd party IP-Core, High-Level Synthesis	Debug, HighLevel SIM, Co-Simulation
Digital Logic	FSM, control- and dataflow	VHDL, Verilog, SystemVerilog	RTL Simulation, Logic Analyzer
I/O	LVTTL, LVDS, MGT	VHDL, Verilog, Dynamic Reconfiguration Ports	Eye diagrams, Network Analyzer, Oscilloscope

Contact Information

Missing Link Electronics
www.MLEcorp.com

Endric Schubert
endric@MLEcorp.com
Phone US: +1 (408) 320-6139
Phone DE: +49 (731) 141149-66