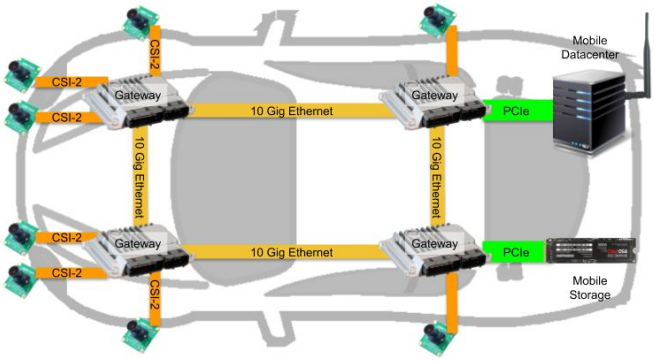
Automotive Zone Gateway Connectivity with PCIe and TSN

Patent pending technology integrates IEEE Standards for Time-Sensitive Networking with Heterogeneous Packet Tunneling for PCIe and others. Protocol Full-Accelerators deliver 10 Gbps linerates, or faster.

Available as a complete hardware / software system stack based on 3rd party IP from German Fraunhofer for FPGA and ASIC implementations.

Application Use Cases

- Zone-Based Automotive Backbone
- High-Speed Automotive Connectivity for Heterogeneous Real-Time Networking
- Automotive Test Equipment for PCIe



Realtime Ethernet Compliance

- Time Sync IEEE 802.1AS (IEEE 1588 profile)
- Bounded Low Latency
  IEEE 802.1Qav Credit Based Traffic Shaper
  IEEE 802.1Qbu / 802.3br Preemption
  IEEE 802.1Qbv Scheduled Traffic
  IEEE 802.1Qcr Async Traffic Shaping
- Reliability: IEEE 802.1Qca Path Control, IEEE 802.1CB Frame Replication & Elim.
- Dedicated Resources & API
  IEEE 802.1Qat Stream Reservation
  IEEE 802.1Qcc TSN Config
  IEEE 802.1CS Link-Local Reservation

Deliverables

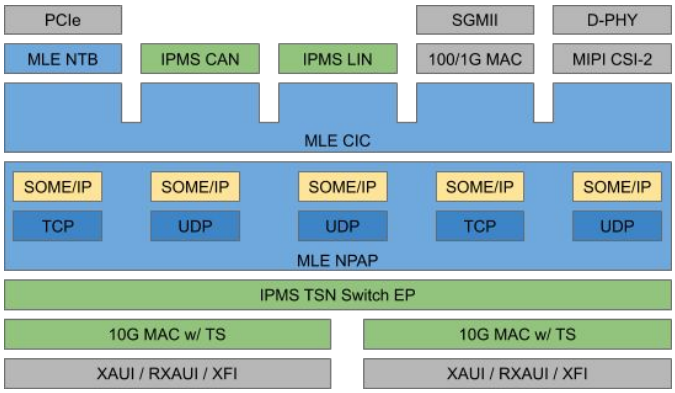
- Commercial Product License for ASIC/FPGA
- Customized, integrated turnkey solutions
- Application-specific expert design services

Key Features

- PCI-SIG Base Spec 3.1 or 4.0 compliant
- PCIe scales from Gen1 x1 to Gen4 x8
- TCP/UDP/IP IETF 1122 compliant
- Network scales to 10/25/50 Gbps
- Supports low-latency tunnels for PCIe sideband signals (INTx, PERST)
- Uses PCIe AER and DPC to integrate w/ Functional Safety watchdogs
- Optional ARM OP-TEE based security

Exemplary System Stack

- PCIe Endpoint and Root-Port in FPGA/ASIC
- PCIe Switch in FPGA/ASIC
- PCIe NTB in FPGA/ASIC
- TCP/UDP/IP over TSN in FPGA/ASIC
- netdev Linux Device Drivers



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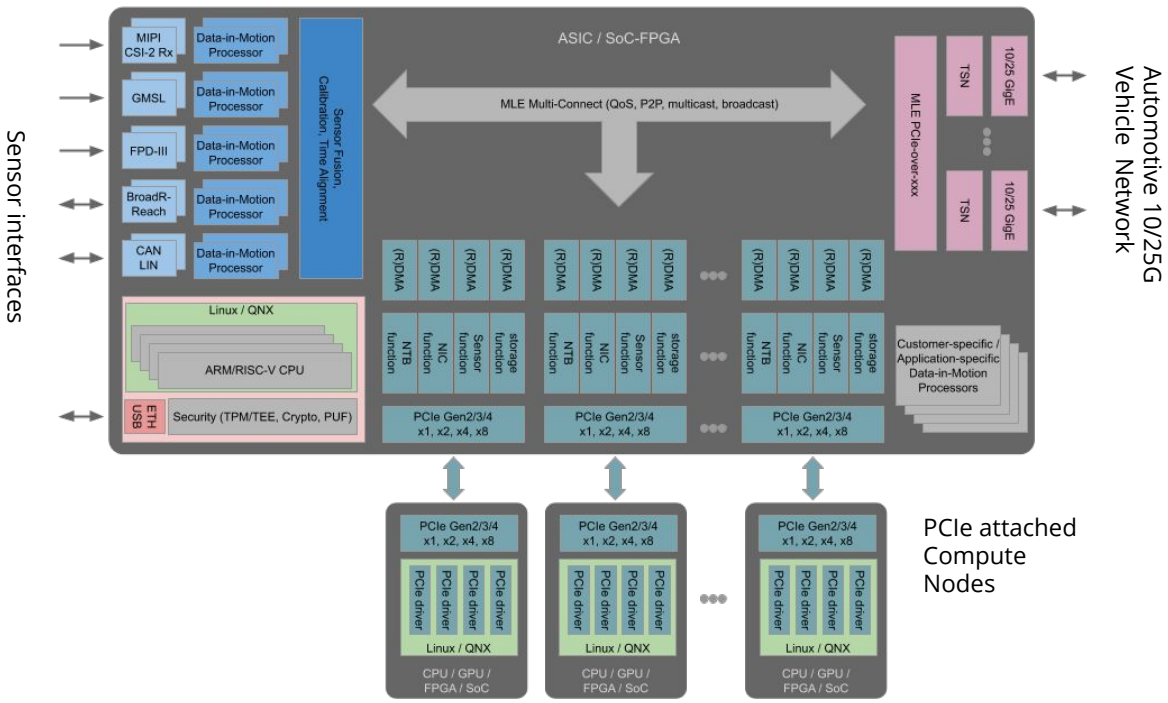
Example Block Diagram



Technology Backgrounder

- Time-Sensitive Networking (TSN) / IEEE 802.1 standardized “Real-time Ethernet” https://www.ipms.fraunhofer.de/de/research-development/wireless-microsystems/ip-cores/tsn.html
- PCIe Non-Transparent Bridging: PCI-SIG standardized high-bandwidth, low-latency ECU-layer CPU/GPU/SoC connectivity https://members.pcisig.com/wg/PCI-SIG/document/13089
- PCIe Long-Range Tunneling: Transporting standard PCIe over OSI Layers 5 https://mlecorp.com/files/papers/04_10_PCIe_Range_Extension_via_Robust_Long_Reach_Protocol_Tunnels_UL.pdf
- TCP/UDP/IP Full Accelerator: Reliable TCP/UDP/IP protocol accelerator with high-bandwidth and deterministic low-latency https://mlecorp.com/npap

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