PCIe-over-TCP-over-TSN-over-10/25GigE

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Presentation at "Programmable Processing for the Autonomous / Connected Vehicle" Sep-24 2020

https://innosued.de/workshop-programmable-processing-for-the-autonomous-connected-vehicle/



Outline

WHY

Automotive needs 10 Gig networking, or more! Electric vehicles and ADAS / Automated Driving
push the migration from Domain-based over to Zone-based Architectures, which again pushes
for more bandwidth and real-time capabilities in the Automotive Network.

WHAT

• Out patent pending technology integrates IEEE Standards for Time-Sensitive Networking with Heterogeneous Packet Tunneling for PCIe, 100Base-T1, MIPI CSI-2, CAN-FD, and others. Utilizing Protocol Acceleration in hardware we can scale to 10 Gbps linerates, and beyond.

HOW

A Software and Semiconductor IP core subsystem which integrates 3rd party IP from German
 Fraunhofer with technology from MLE and can be licensed for FPGA and ASIC implementations.



Backgrounder Missing Link Electronics

Our Mission is to

- Apply FPGA technology for Domain-Specific Architectures
- Offer pre-validate FPGA subsystems of FPGA IP blocks and open-source software
- Support customer projects with deep expertise and hands-on design services

Head-quartered in Silicon Valley with Design Offices in Germany

- Founded 2010, employee owned
- 15+ Certified FPGA Designers
- 50+ Presentations at Technology Conferences, 4 Patents

Technology Partnerships



















Our Technology Achievements

- Patented technology in the fields of networking, mixed-signal, functional safety
 - US Patent 9,209,828 Configurable Mixed-Signal Systems
 - US Patent 10,140,049 Partitioning Systems Operation in Multiple Domains
 - US Patent 10,509,880 Automation for Configurable Mixed-Signal Systems
 - o US Patent 10,708,199 Heterogeneous Packet-Based Transport
- 50+ Presentations at Technology Conferences and in Technology Journals
 - Embedded World Conferences
 - PCI-SIG Developers Conferences
 - o IBM Open Power Summit
 - SNIA Storage Developers Conferences
 - Flash Memory Summits
 - Xilinx XCELL Magazines
 - XILINX Developer Forum and Security Workshops



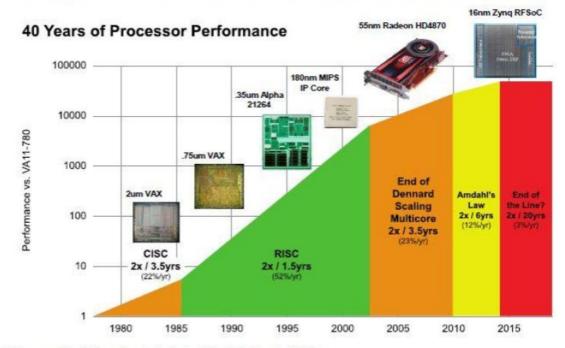


Domain-Specific Architectures

FPGAs as a very powerful processor that executes "dataflow software"

Apply HPC/HA Datacenter technology to other verticals - "Proudly borrowed elsewhere!"

Challenges: The End of Moore's Law and Scaling



Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e 2018



Our FPGA Design Expertise

- Mentor, Cadence, Xilinx Toolflows
- Zynq-7000 SoC in designs since Q1/2012
- Zyng Ultrascale+ MPSoC in designs since Q4/2015
- Zyng UltraScale+ RFSoC in designs since Q2/2018
- PetaLinux / Vanilla Linux and Yocto-based SW development
- Multigigabit transceiver configurations
 - PCIe Gen2/3/4, SATA 3/6G, SAS 6/12G, NVMe,
 - CAPI, JESD204B, DP/HDMI, MIPI CSI-2 D-PHY
 - o 10/25/4050/100G Ethernet, Low Latency Ethernet
- Radar, civil, mil/aero, automotive
- camera, Lidar, data recording
- Functional Safety Design Flows ISO 26262 (ASIL), IEC 61508 (SIL)
- Security & Trust
 - o PUF, Crypto, Trusted Execution Environment, OP-TEE







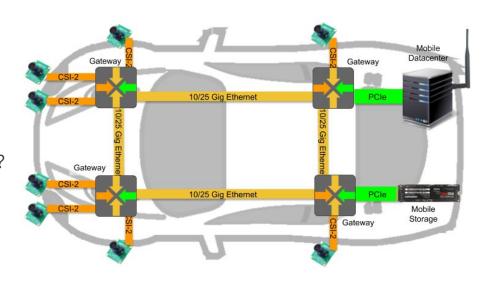
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Zone-Based 10 GigE Automotive Backbone

Do you ...

- Prefer open IEEE standards over closed proprietary ones?
- Need 10+ Gbps bandwidth?
- Need deterministic, low-latency real-time network behavior, namely TSN?
- Need heterogeneous connectivity with PCIe, 100Base-T1, MIPI CSI-2, CAN-FD, etc?
- Need Functional Safety and Security / Hardware Root-of-Trust?

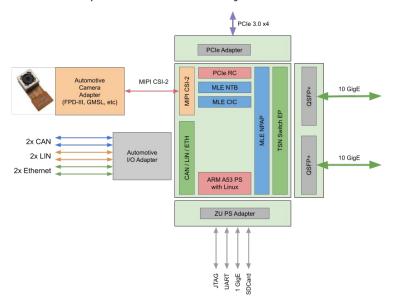
⇒ Use time-to-market solutions from MLE 100% "Made-in-Germany"



MLE LabCar for "Tunneling" PCIe (and else)

FPGA-based Prototyping System for Architecture Exploration and Development

Example of Zone Gateway Node



- Commercial Product License for FPGA or ASIC implementation
- Sign-once License for complete subsystem including 3rd party IP
- Customization NRE fee



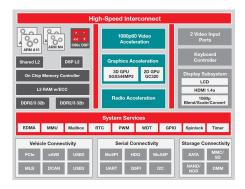
- Prototyping example:
 4-node "Lab Car", incl. Hardware, Software,
 Firmware and licenses for in-house evaluation
 and FPGA development
- **⇒** Use time-to-market solutions from MLE 100% "Made-in-Germany"

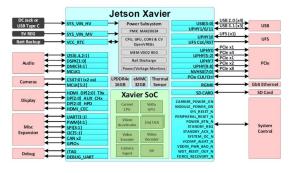


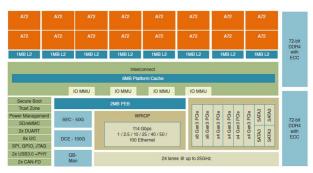
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Why PCIe?

- Future-proof road-map, driven by PCI-SIG
- PC, Cloud Computing, Embedded Systems drive this roadmap
- Best-in-class price (\$) per performance (Gbps) ratio
- Modern automotive SoCs all support PCIe









Why Ethernet?

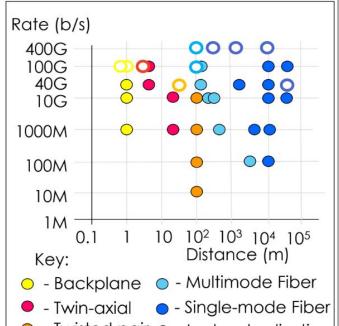
- Future-proof road-map, driven by PCI-SIG
- PC, Cloud Computing, Embedded Systems drive this roadmap
- Best-in-class price (\$)
 per performance
 (Gbps) per length
 (meters) ratio

Distance vs Speed



Ethernet operates at different speeds over different distances depending on the media:

- backplanes up to 1m
- Twinax to 15m
- Twisted pair to 100m
- Multimode fiber to 5km
- Single-mode fiber to 40km

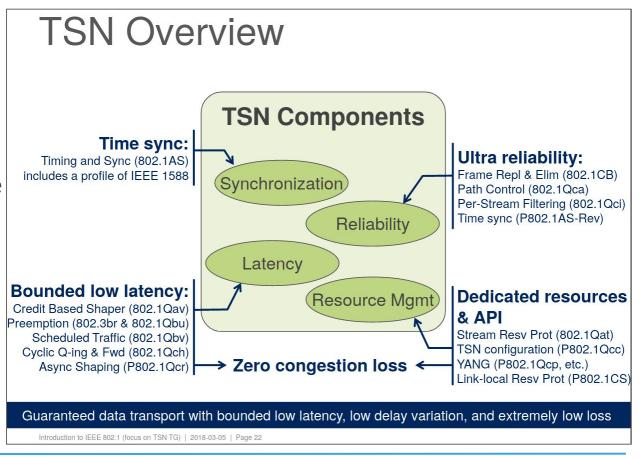


Twisted pair O - In standardization



Why TSN?

- IEEE open standard for real-time networking
- Telco and Datacenter drive the roadmap





Unique Technology Combination

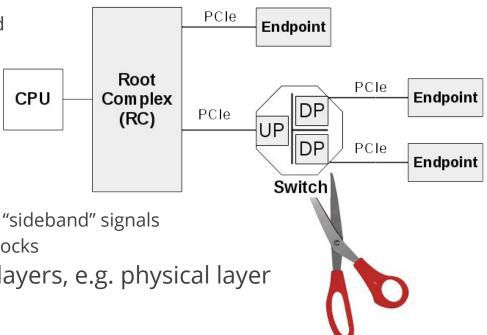
- 1. PCIe Range Extension via Robust, Long-Range Protocol Tunnels
- 2. PCle Non-Transparent Bridging (NTB)
- 3. PCle / NVMe Full Acceleration
- 4. TCP/UDP/IP Full Acceleration (Fraunhofer HHI)
- Time-Sensitive Network IP (Fraunhofer IPMS)
- ⇒ Real-Time Multi-Protocol Heterogeneous Packet-Based Transport

Licensed by other Xilinx customers as Platform Subsystem



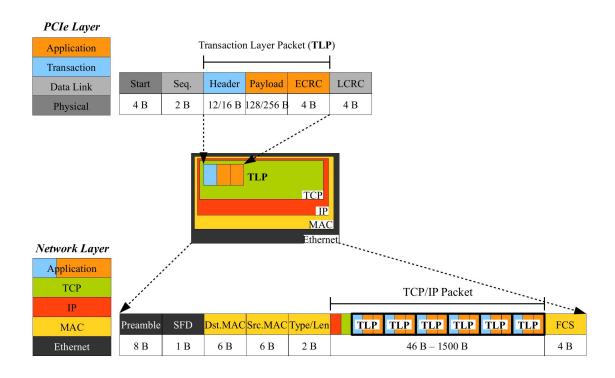
PCIe Range Extension via TCP/IP

- Fully transparent to network equipment
 - Just a bunch of TCP sessions
 - No special traffic handling required
- Fully transparent to PCIe
 - Reliable transport via TCP
 - Congestion control via TCP
- A "distributed" PCIe Switch
 - In accordance to PCle Spec
 - Scalable via TCP session count
 - Supports latency requirements for "sideband" signals
 - Special care needed to avoid deadlocks
- Independent of lower network layers, e.g. physical layer



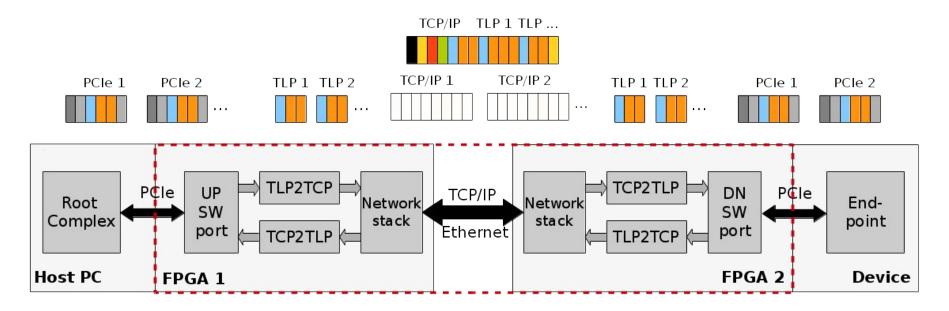


Concept of PCIe-over-TCP (1)





Concept of PCIe-over-TCP (2)



---- Distributed PCIe Switch



TCP/UDP/IP Full Accelerator

- "Packet Processing" in hardware (FPGA/ASIC)
 - Low latency in microseconds
 - Deterministic (no CPU, no cache misses)
 - Performance scales to 100 Gbps
- In accordance to IETF RFC 1122

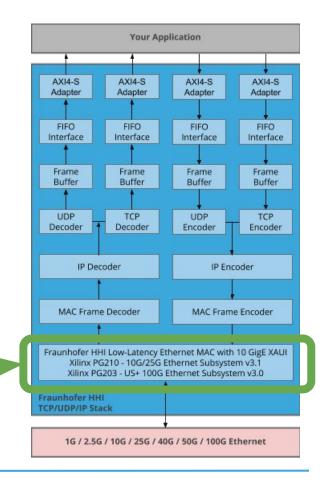
Mature technology licensed from Fraunhofer HHI



Heinrich Hertz Institute

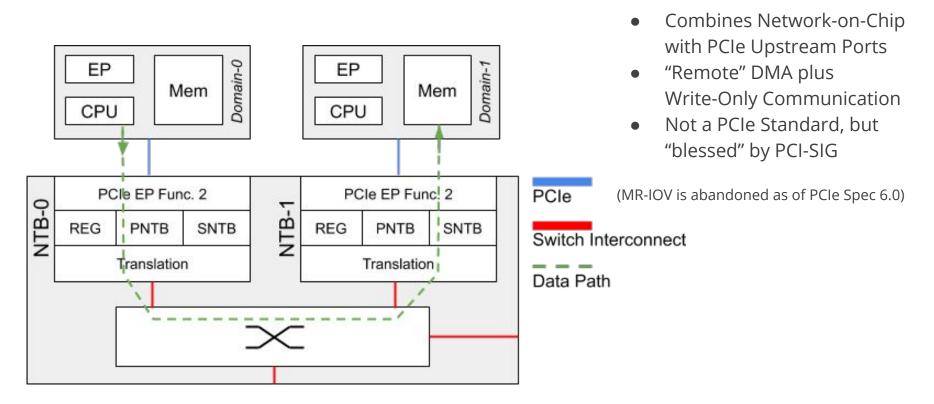
Extensible Real-Time Behavior via TSN MAC





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PCIe NTB - enables CPU-to-CPU Direct Comm

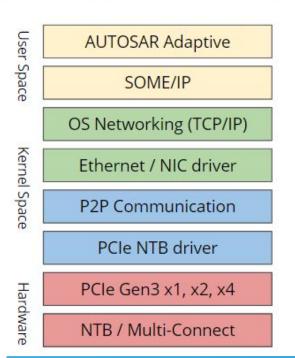




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PCIe NTB - Via Well Known Network API

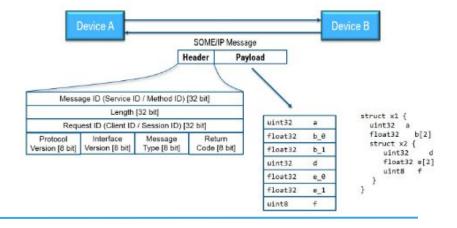
Software Stack on Compute Node (Linux, QNX, Adaptive AUTOSAR, ...)



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Application Programmer's View

- Fully transparent comm. via PCIe NTB
 - Local (within one ECU)
 - Remote (between multiple ECUs)
- IP address for each Compute Node
- Gateway does routing, fail-over re-routing
- Send/receive TCP/IP, UDP/IP, SOME/IP messages



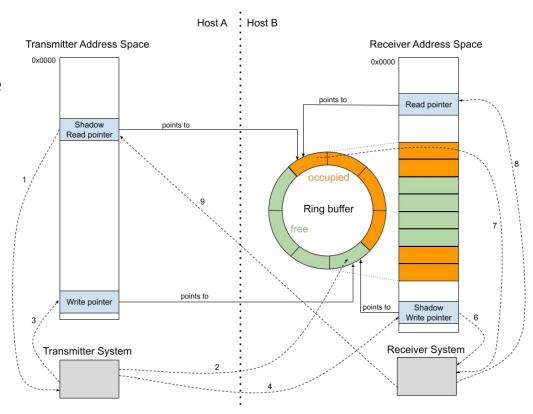


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PCIe NTB High Performance Delivered

- Write-Only Comm via Doorbells and PCle Posted Writes
- Avoids difficulties of PCIe multi-device
- Scales to > 32 PCle RCs

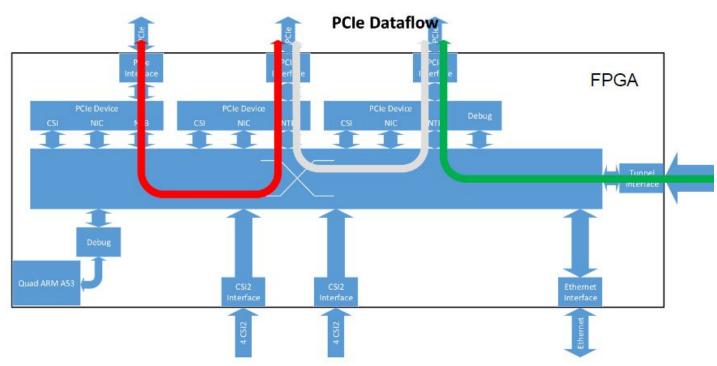
"Borrowed" from NVMe Spec





Network of PCIe - Onchip, Offchip, Backbone

Custom Switch Based Design





Platform Technology Example

Fully integrated system stack for automotive connectivity

• Available for ASIC and/or FPGA implementation

TSN Features:

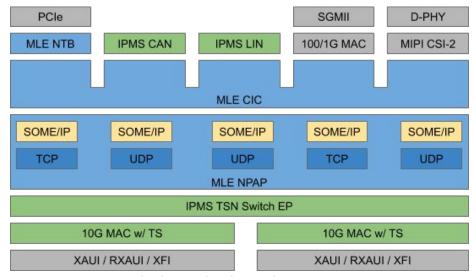
- IEEE 802.1AS, 802.1Qav, 802.1Qbv, 802.1Qci, 802.1Qcb
- Switch and Endpoint mode
- Scales to 10/25 Gbps

TCP/UDP/IP Features:

- IETF RFC 1122 Supported
- Autosar 4.x SOME/IP accelerated
- Scales to 10/25/50/100 Gbps

PCle Features:

- PCI-SIG Base Spec 3.1 or 4.0 using x1, x4, x8
- Scales to 8/16/32/64/128 Gbps

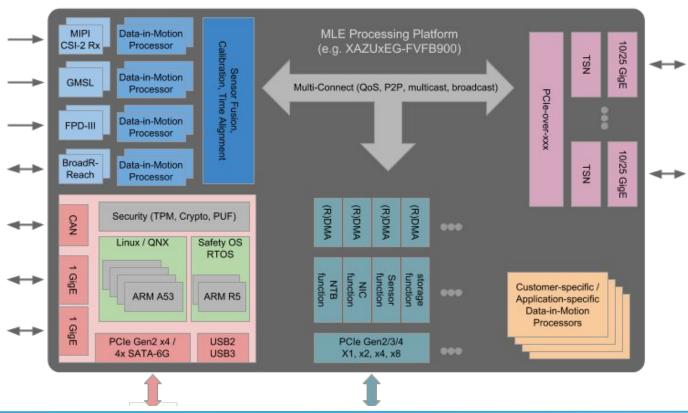


System-level protocol stack example



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Implementation with Xilinx FPGA

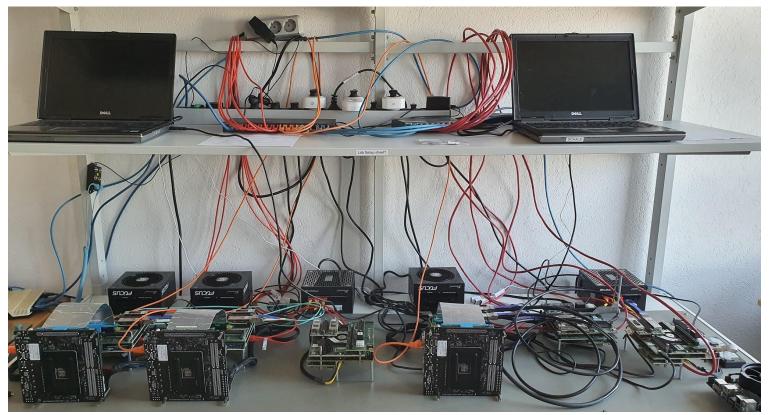




Ongoing Research & Development w/ Partners

- Functional Safety (apply PCIe aspects for High-Availability)
 - Watchdog for PCIe AER (Advanced Error Reporting)
 - PCle DPC (Downstream Port Containment)
 - IEEE 802.1CB (Frame Replication / Elimination)
- Security
 - PCIe RC/EP Authentication
 - ARM Secure OP-TEE
- Real-Time Behavior
 - IEEE 802.1AS and PCIe PTM



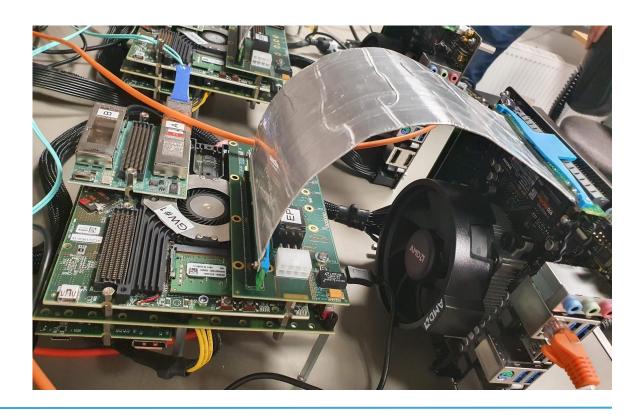




Uses ASIC Emulators from ProDESIGN GmbH

"LEGO"-like interface boards for

- PCle
- 10/25G Ethernet
- etc



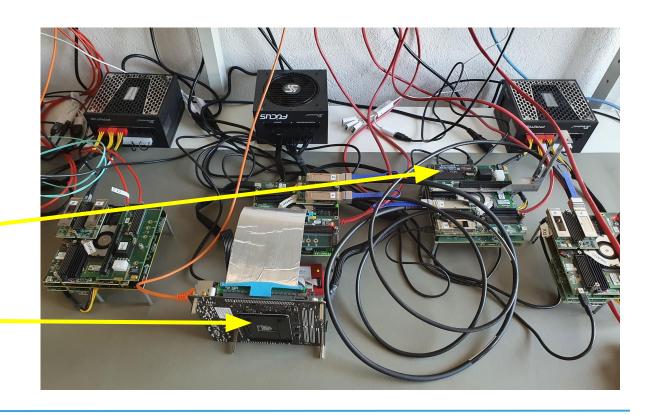


Backbone with 2 FPGA Gateways

for PCle-over-...

to m.2 NVMe SSD

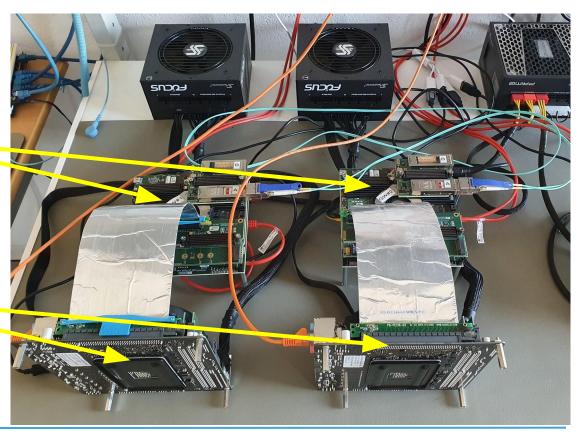
from mini-ITX PC



Backbone with 2 FPGA Gateways

for PCIe NTB

between 2 mini-ITX PCs





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