



Zone-Based Automotive-Backbones

Automotive Ethernet Congress

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Fraunhofer IPMS

IP Cores, ASIC & FPGA Design

- Xilinx, Intel/Altera, Microsemi, Lattice and tool support
- IP Core, SoC & high speed datacomm design
- Serdes integration up to 200Gbps
- Simulation, verification & board level test

FPGA Design

Silicon Design

ASIC

- Down to 22nm
- Digital, mixed signal, RF (up to 60 GHz)
- Frontend, Backend, Floorplanning & Sign-off
- CADENCE driven tool chains (Synopsys & Mentor Graphics partly)
- Simulation, verification, IC & board level test

Concept, IP core & SoC design

- HAL, firmware, driver development, SDK, Continuous Delivery (CD)
- FreeRTOS, Linux integration
- ISO26262 functional safety, ASIL-B and ASIL-D ready IP cores

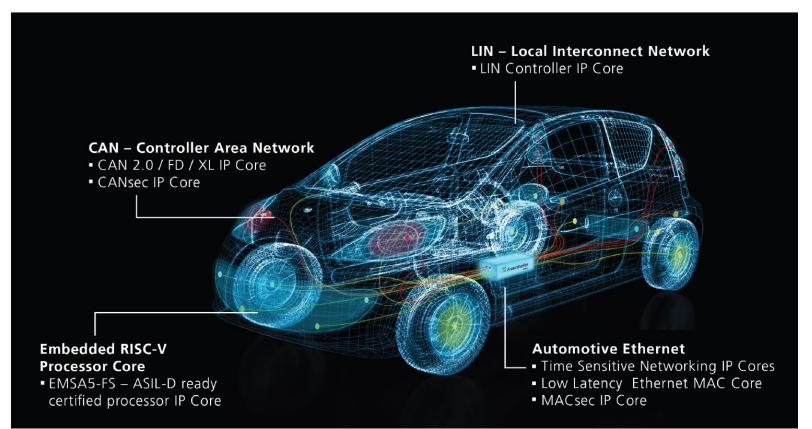
General





IP Cores from Fraunhofer IPMS

Overview





Missing Link Electronics

Mission: "If It Is Packets, We Make It Go Faster!"

High-Performance (Embedded) Compute & Connected Systems-of-Systems

- PCIe (CXL, ISB, NVMe)
- Ethernet (TCP/IP, TSN)
- Audio/Video (HDMI, SDI)



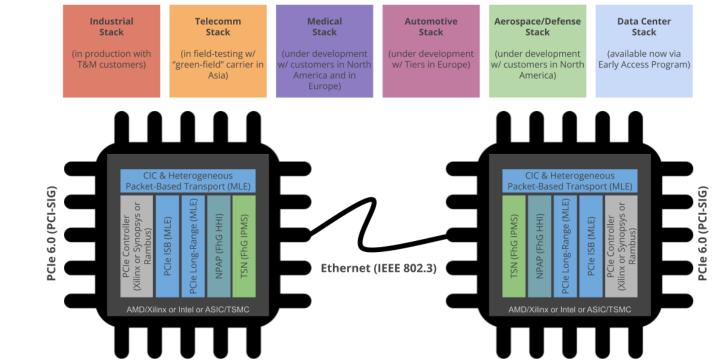


Foundation Technology With Many Applications

Implemented as a unique IP combination from Fraunhofer and MLE

Built on top of open standards from PCI-SIG and IEEE

Implemented in ASIC and FPGA





missing link electronic

Fraunhofer IPMS + Missing Link Electronics

Partnership

- Fusing expertise in
 - Ethernet
 - TSN
 - PCle
 - Automotive enabled design
- Aim
 - Zone based Automotive Backbones
 - Enabling future Automotive network architectures
 - Saving costs on wiring





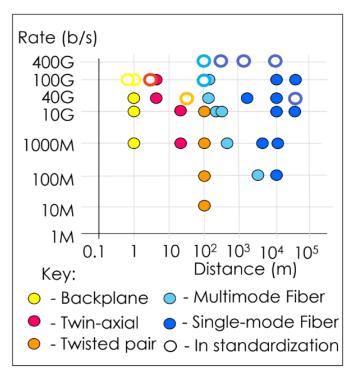
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Why Ethernet?

- Distance vs Speed
- Future-proof road-map
- PC, Cloud Computing, Embedded Systems drive this roadmap
- Best-in-class price (\$) per performance (Gbps) per length (meters) ratio

Ethernet operates at different speeds over different distances depending on the media :

- backplanes up to 1m
- Twinax to 15m
- Twisted pair to 100m
- Multimode fiber to 5km
- Single-mode fiber to 40km







ethernet alliance

Why PCIe?

- Future-proof road-map, driven by PCI-SIG
- PC, Cloud Computing, Embedded Systems drive this roadmap
- Best-in-class price (\$) per performance (Gbps) ratio
- Common to modern SoCs, ability to commoditize silicon

High-Speed Interconnect										
				1080p60 Video Acceleration				2 Video Input Ports		
Shared L2 DSP L2				Graphics Acceleration				Keyboard Controller		
On Chip Memory Controller				s	3D GPU GX544MP2	2D GPU GC320		Display Subsystem		
L3 RAM w/ECC DDR2/3 32b DDR2/3 32b				Radio Acceleration				HDMI 1.4a 1080p Blend/Scale/Convert		
System Services										
EDMA	MMU	Mailbox	RT	C	PWM	WDT	GPIO	Spinlock	Timer	
Vehicle Connectivity			1	Serial Connectivity				Storage Connectivity		
PCle	eAVB	USB2	McSPI HDQ McASP SATA MMC/ SD							
MLB	DCAN	USB3	UART QSPI I2C NAND/ DMM					DMM		

DC lack or		Jetson Xavier			
USB Type C 5V REG		Power Subsystem PMIC MAX20024	USB[3:0] UPHY1/6/11	(USB 3.1 (x3))	USB
Batt Backup		CPU, GPU, CORE & CV OpenVREGs	UPHY10 UFS CLK/RST UPHY0	PCle x1	UFS
Audio	 I2S[6,4,2:1] DSPK[1:0] DMIC[4:1] MCLK1 	MEM VDD2 REG Rail Discharge Power/Voltage Monitors	UPHY[5:2] UPHY[7 UPHY[9:8] NVH50[7:0]	PGe x1 PGe x2 PGe x8	PCle
Cameras 🖌	CSI[7:0] (x2 ea) MCLK[5:2]	LPDDR4x eMMC Thermal 16GB 32GB Sensor	PCIe CLK/Ctrl RGMII	\leftarrow	Gbit Ethernet
Display	HDMI DP[2:0] TXx DP[2:0] AUX CHx DP[2:0] HPD HDMI_CEC	Xavier SoC	SD CARD CARRIER_POWER_ON MODULE_POWER_ON SYS_RESET_N	← →	SD Card
Misc Expansion	UART[3:1] PWM[4:1] \$P[[3:1] 12C[5:1] CAN x2 GPIOs	Vision Accelerator Video Encoder Video Decoder	PERIPHERAL_RESET_N POWER_BTN_N STANDBY_REQ STANDBY_ACK_N SYSTEM_OC_N VCOMP_ALERT_N	\longleftrightarrow	System Control
Debug		Camera Ingest	VDDIN_PWR_BAD_N WDT_RESET_OUT_N FORCE_RECOVERY_N		







Zone-Based Automotive Backbone

Why TSN?

- Time Sensitive Networking
- The history
 - AVB Task Group for latency free delivery of audio/video data
 - 2012 the TSN Task Group evolved from the AVB Task Group (IEEE 802.1)
- TSN is not a single standard
- It's a collection of sub standards and extensions
 - Network wide time synchronization
 - Determinism
 - Low latency
 - Low jitter
- Scalable speed





TSN profiles & standards

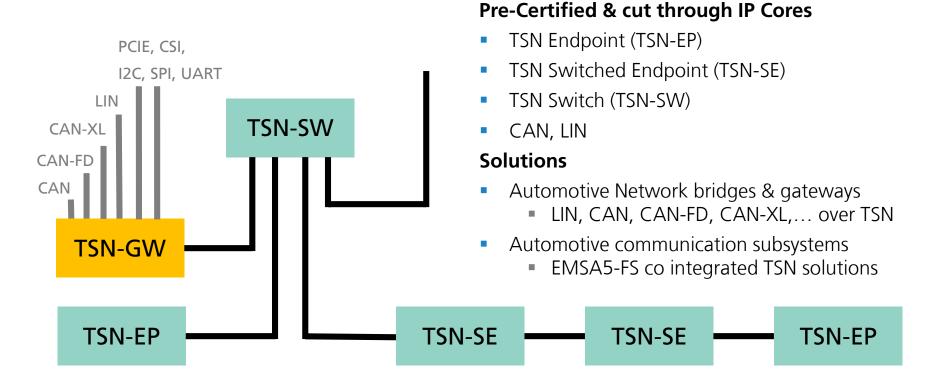
Overview

- Standards
 - Time Synchronization (802.1AS & it's profile IEEE 1588, 802.1AS/-2020)
 - Bounded low latency (802.1Qav, 802.1Qbv, 802.3br & 802.1Qbu, 802.1Qch, P802.1Qcr, P802.1Qcr, P802.1DC..)
 - High availability/reliability (802.1CB, 802.1Qci, 802.1Qca)
 - Resources and API (802.1Qat, 802.1Qcc, 802.1Qcp, P802.1Qcx, P802.1ABcu, P802.1Qcw, 802.1CBcv, P802.1CS, P802.1Qdd, P802.1CBdb..)
- Profiles
 - Audio Video Bridging (802.1BA)
 - Fronthaul (802.1CM)
 - Industrial Automation(IEC/IEEE P60802)
 - Automotive In-Vehicle (P802.1DG)
 - Service Provider (P802.1DF)
 - TSN for Aerospace Onboard Ethernet (P802.1DP)
 - TSN for Avionics (SAE AS-1A2*)



TSN IP Cores from Fraunhofer IPMS

Overview

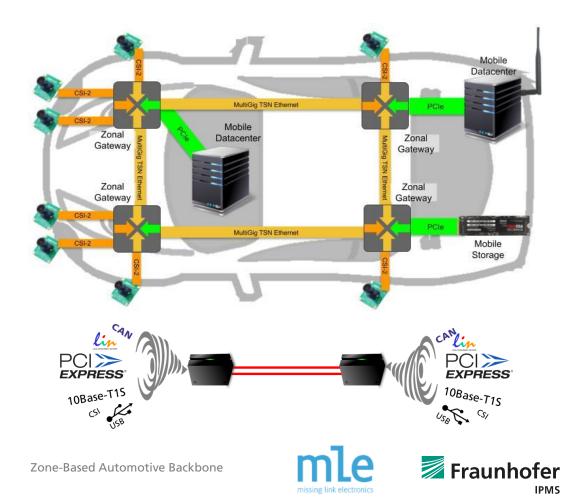




Automotive functional safety enhanced backbone

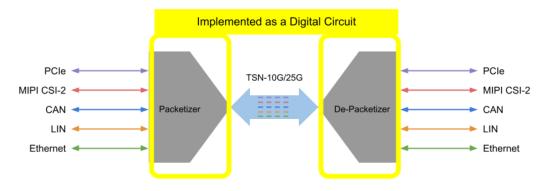
Architectural approach

- Discrete Gateways
- Integrated Gateways
- Multi protocol tunneling
- High bandwidth
- Realtime
- Low latency
- Low jitter



Automotive functional safety enhanced backbone

TSN-GW zonal gateway ... Multi Protocol Tunneling



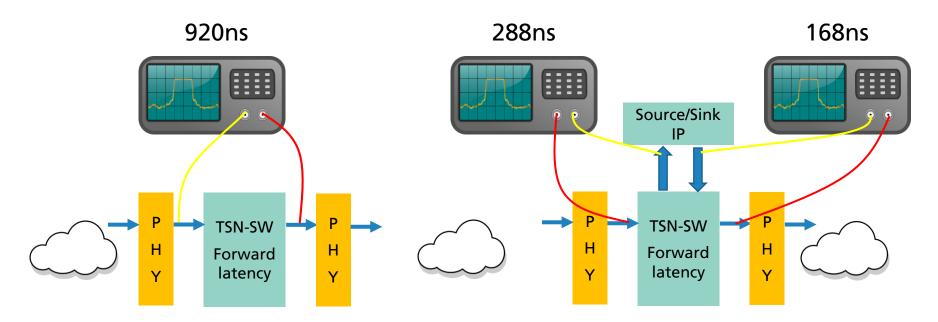
- Tunneling
 - Packetizing/Enveloping data
 - Tunneling via redundant TSN backbones
 - Maintaining real time and latency requirements
 - De-packetizing/De-enveloping data
- Multi-Protocol Switching
 - Repackaging
 - Switching



Latency

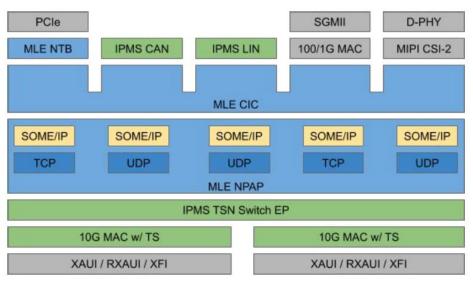
Forward & Injection latency TSN-SW

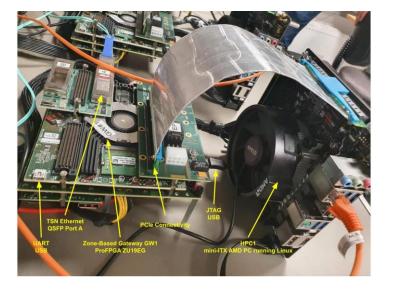
FPGA (Cyclone V SoC)





Automotive functional safety enhanced backbone PCIe Protocol Tunneling





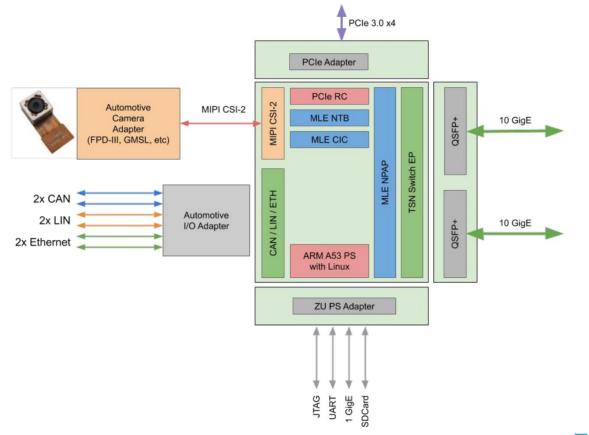
- PCIe Endpoint and Root-Port in FPGA/ASIC
- PCIe Switch in FPGA/ASIC
- PCIe NTB in FPGA/ASIC
- TCP/UDP/IP over TSN in FPGA/ASIC
- netdev Linux Device Drivers





Automotive functional safety enhanced backbone

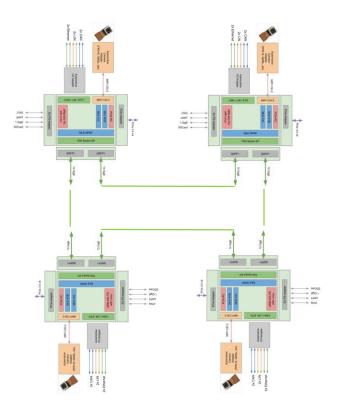
LabCar for parallel tunneling automotive protocols





Automotive functional safety enhanced backbone

LabCar for tunneling automotive protocols







IPMS

Summary

Zone based Automotive Backbones



- TSN is a good solution for tunneling all kinds of time critical communication
- TSN can cope with huge network loads while maintaining real time requirements
- Cut-Through IP is the best choice for ultra low latency networks
- TSN is defined by open IEEE standards
- TSN is scaling with the evolution of Ethernet
- PCIe offers high performance and superior integration
- Fraunhofer IPMS is your partner for custom TSN Solutions
- MLE provides High-Performance (Embedded) Compute & Connected Systems





Contact Information

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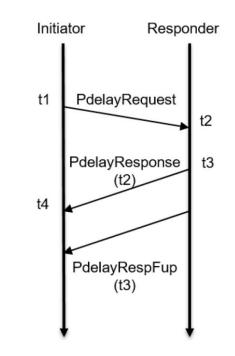


BACKUP



Time synchronization - IEEE 802.1AS (AS-2020)

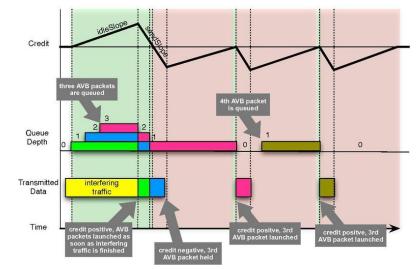
- Network wide operation
- Non 802.1as capable devices break up network
- Periodic announce messages
- Grand Master (GM) is selected for device with the best master clock algorithm (BMCA)
- Periodical Sync + Followup frames
- delay measurement is a two-step peer-to-peer path delay algorithm





IEEE 802.1Qav - Credit Based Shaper

- Forwarding and Queuing Enhancements for Time-Sensitive Streams
- Allready used in AVB
- Credit based scheduling
- Positive credit allowing traffic to be sent
- Negative credit will prevent packets to be send

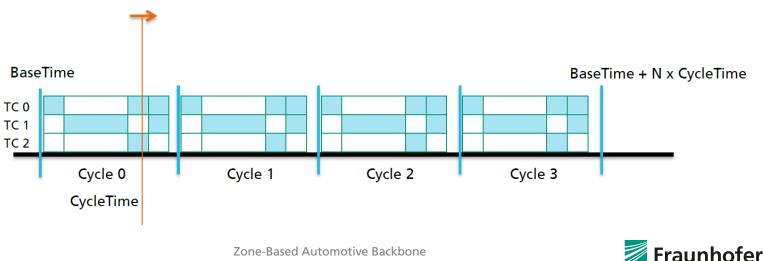


Source: https://en.wikipedia.org/wiki/File:Traffic-shaping.pdf



IEEE 802.1Qbv - Time Aware Shaper

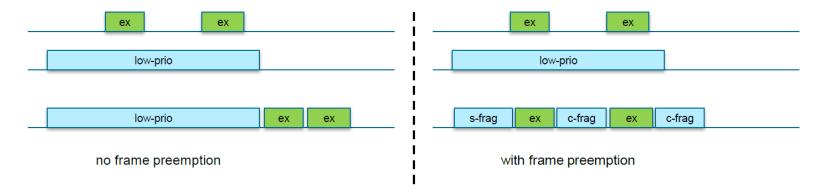
- Cycle based scheduling of frames
- Cycle length
- A number of gate operations
- Guard bands prevent violation of cycle timings



Zone-Based Automotive Backbone

802.3br & 802.1Qbu – Frame preemption

- Extreme low latency for chosen traffic (express traffic)
- Special mPackets (express packet, preemptable packet, fragment of a packet)
- 64bytes of minimal fragment size





IEEE 802.1CB - Frame replication and elimination for redundancy

- Sequence generation
- Split/Recovery
- Redundancy tag seq encode/decode
- Stream identification
- Link aggregation (802.1AX)

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Upper layers	· · · · · · · · · · · · · · · · · · ·			
Sequence generation function (7.4.1)	Upper layers			
Stream splitting function (7.7)	Sequence recovery function (7.4.2)			
Sequence encode decode function (7.6)	Sequence encode/decode function (7.6)			
Stream identification function (6.2)	Stream identification (6)			
IEEE 802.1AX Link Aggregation	IEEE 802.1 Link Aggregation			
мас мас	MAC			
	Ри́У Ри́У			
VVV				



IEEE 802.1Qci – Per-Stream Filtering and Policing (PSFP)

- Filtering and policing and frame queue decisions made on a per-stream basis for received frames
- Stream gate id \rightarrow open/closed

