Zonal / SDV Architecture Exploration From Whiteboard to Vehicle Demo in 9 Months

Automotive Rapid Prototyping in the MANNHEIM CeCaS Project

MLE – Experts for Domain-Specific Compute Architectures

Our Mission: From Software to Silicon!

- Deliver HW and SW for High-Performance (Embedded) Compute Systems & Solutions
- Offering pre-validated subsystems with FPGA IP blocks and open-source software
- Support customer projects with deep expertise and hands-on design services

Head-quartered in Silicon Valley with Design Offices in Germany

- Founded 2010, employee owned
- 20+ Certified FPGA Designers
- Customers include technology leaders, US and European government agencies, Fortune 500 companies
- Partners to:

AMD Adaptive Computing Partner PREMIER

trenz electronic GmbH

PCI SIG

Fraunhofer IPMS

ulm university universität ulm

THU Technische Hochschule Ulm

ELEMASTER

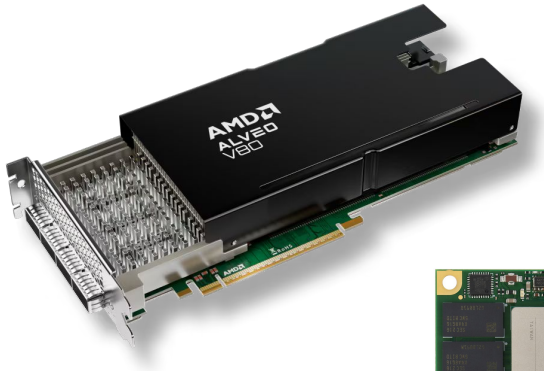
Fraunhofer Heinrich-Hertz-Institut

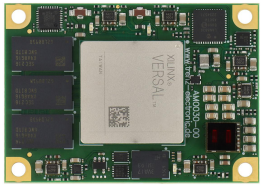
MLE Design Services Expertise – FPGA as a Computer

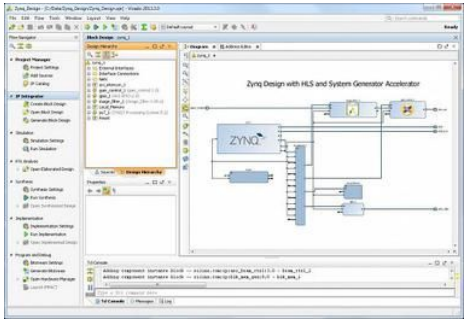
- RTL and High-Level Synthesis using FPGA design flows

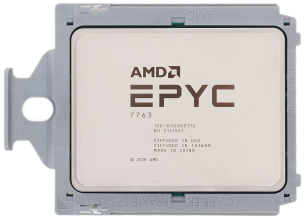
- AMD Zynq-7000 SoC in designs since Q1/2012
- AMD Zynq Ultrascale+ MPSoC in designs since Q4/2015
- AMD Zynq UltraScale+ RFSoC in designs since Q2/2018
- AMD Versal since Q1/2019
- PetaLinux / Vanilla Linux and Yocto-based SW development

- Multigigabit transceiver configurations
  - PCIe Gen2/3/4/5, SATA 3/6G, SAS 6/12G, NVMe, CXL
  - SDI-3/6/12G, JESD204B, DP/HDMI 4k, MIPI CSI-2 D-PHY
  - 10/25/40/50/100G Ethernet, Low Latency Ethernet
- Radar & Lidar for civil, mil/aero, automotive, industrial
- Image processing for HDMI, Displayport, SDI
- Time Sensitive Networking, Detnet, Layer-2/3 Switching
- Functional Safety Design Flows ISO 26262 (ASIL), IEC 61508 (SIL)
- Security & Trust (PUF, Crypto Accelerators , eFuses)









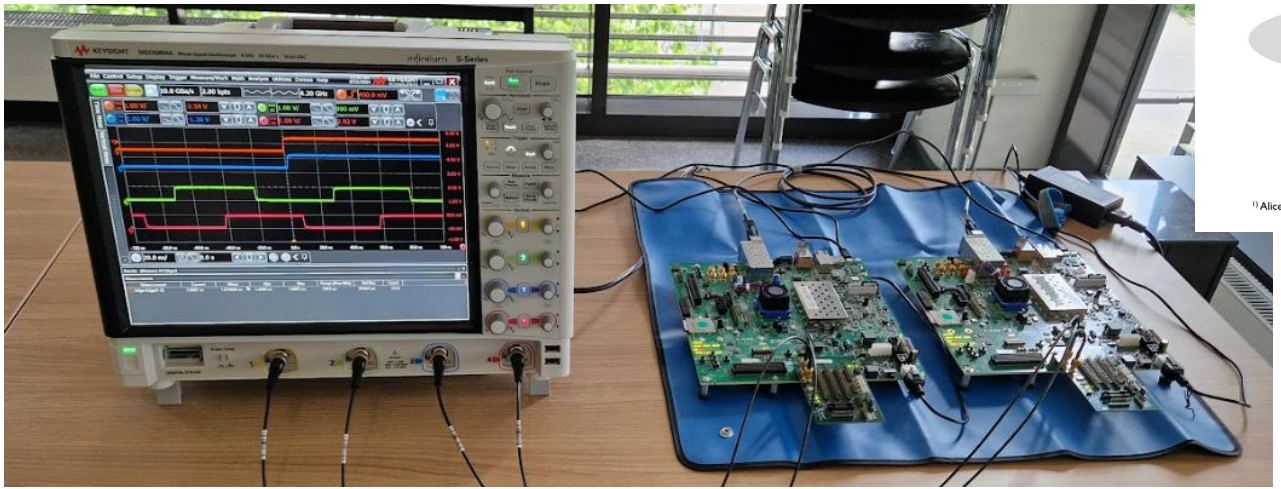
Our Technology Achievements

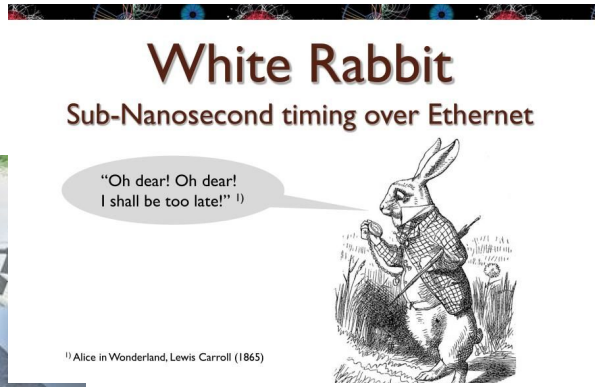
- Patented technology in the fields of acceleration, mixed-signal, functional safety
  - US Patent 9,209,828 – Configurable Mixed-Signal Systems
  - US Patent 10,140,049 – Partitioning Systems Operation in Multiple Domains
  - US Patent 10,509,880 – Automation for Configurable Mixed-Signal Systems
  - US Patent 10,708,199 – Heterogeneous Packet-Based Transport
  - US Patent 10,848,442 – Secure Heterogeneous Packet-Based Transport
  - US Patent 11,356,388 – Real-Time Multi-Protocol Heterogeneous Packet-Based Transport
- 60+ Presentations at Technology Conferences and in Technology Journals
  - Embedded World Conferences
  - PCI-SIG Developers Conferences
  - Flash Memory Summits, SmartNICs Summit
  - FPGA Conferences
  - IBM Open Power Summit
  - Automotive Ethernet Congress
  - XILINX Developer Forum and Security Workshops
  - SNIA Storage Developers Conferences

MLE Technology - Proudly Sourced Elsewhere

Example BMBF VERANO: Koherent digital Radar

MLE optimizes CERN OHL White Rabbit to AMD/Xilinx FPGAs

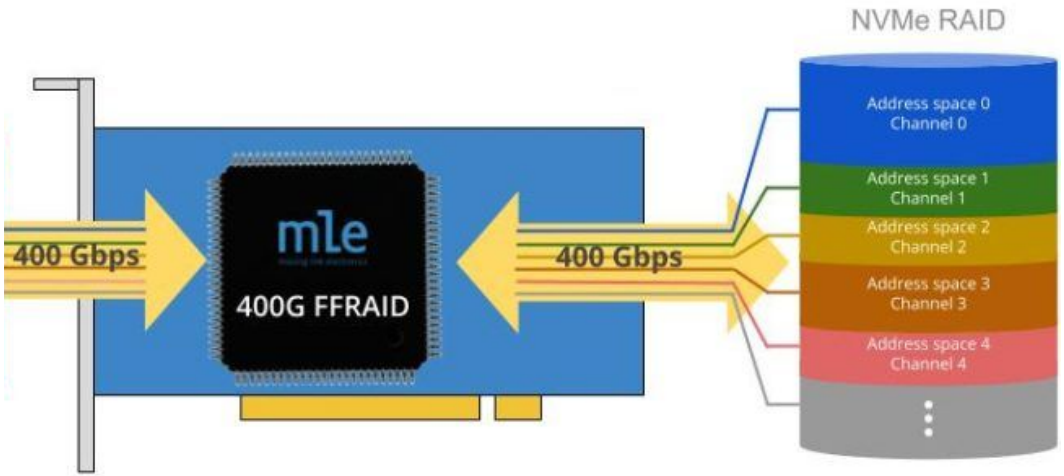




MLE Technology for Automotive

MLE Fast FPGA RAID Storage acceleration for new automotive data logger

- Enables lossless / gapless recording at 200 Gbps (or more)
- Implemented in AMD Alveo U55C



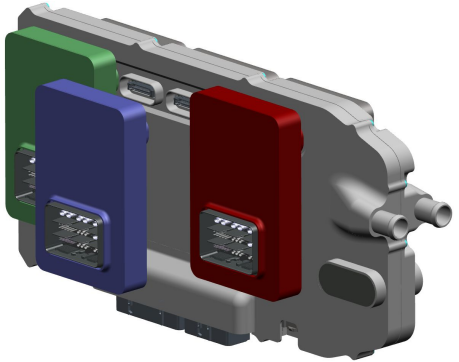
Auto/TSN for Zone Architectures / in-vehicle network

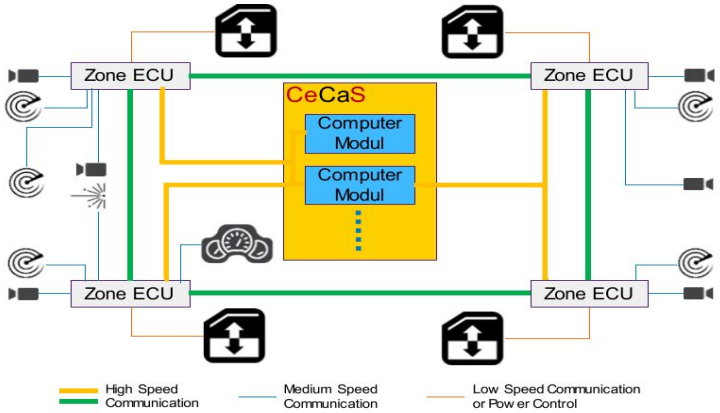
BMBF CeCaS

Budget: 88 Mio EUR

Key Objectives:

- Zone-base architecture
- Auto SoC / Chiplets
- Mechanical / thermal



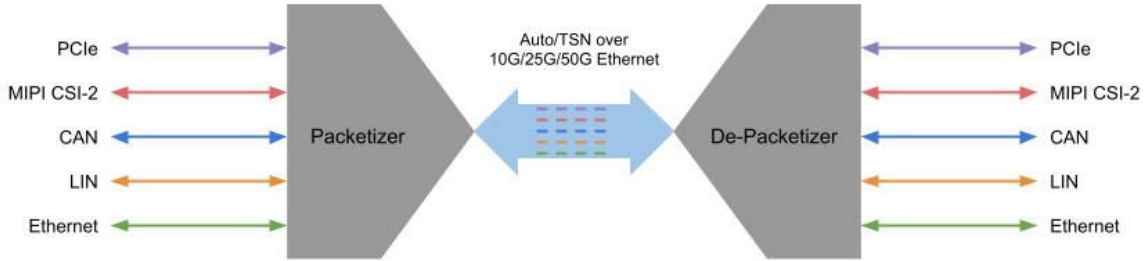


- AMD Versal VM1802 for “emulating” ADAS compute and connectivity
- AMD Versal VE2303 for “emulating” Zone ECUs / gateways

Auto/TSN for Zone Architectures / in-vehicle network

Automotive data over Time-Sensitive Networks, based on open IEEE standards

- Virtualizes in-vehicle network infrastructure
- Full “legacy” connectivity plus enabling “new” high data rate interfaces (PCIe, GMSL, MIPI CSI2)
- Delivers bandwidth, scalability, security, Functional Safety



BOSCH

Multi-Gigabit Automotive Ethernet with AMD Kria KR260 Robotics FPGA Starter Kit

Nov 23, 2023 | 7 Months Ago

AMD's Kria KR260 Robotics Starter Kit builds on the success of AMD's Kria System-on-Modules (SoM) and is an ideal platform to test ideas for multi-Gigabit networking. Because Kria KR260 integrates...

MLE Auto/RPS

Application is for SDV / Zonal Architectures:

- Data-centricity shifts SW development focus from signal to data
- API-first to de-couple and abstract based on vehicle data model
- Modularity & autonomy to enable flexible, scalable SW with high re-use

⇒ Focus on Software Engineers

⇒ Full FPGA System Stack, Ready-to-Run

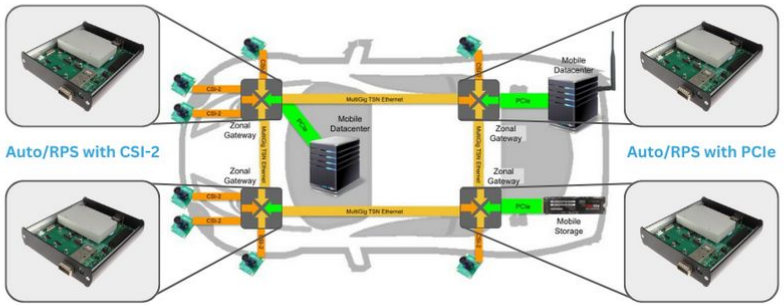
⇒ FPGA is fully transparent (don't have to touch, unless you want to)

Automotive Rapid Prototyping System (Auto/RPS)

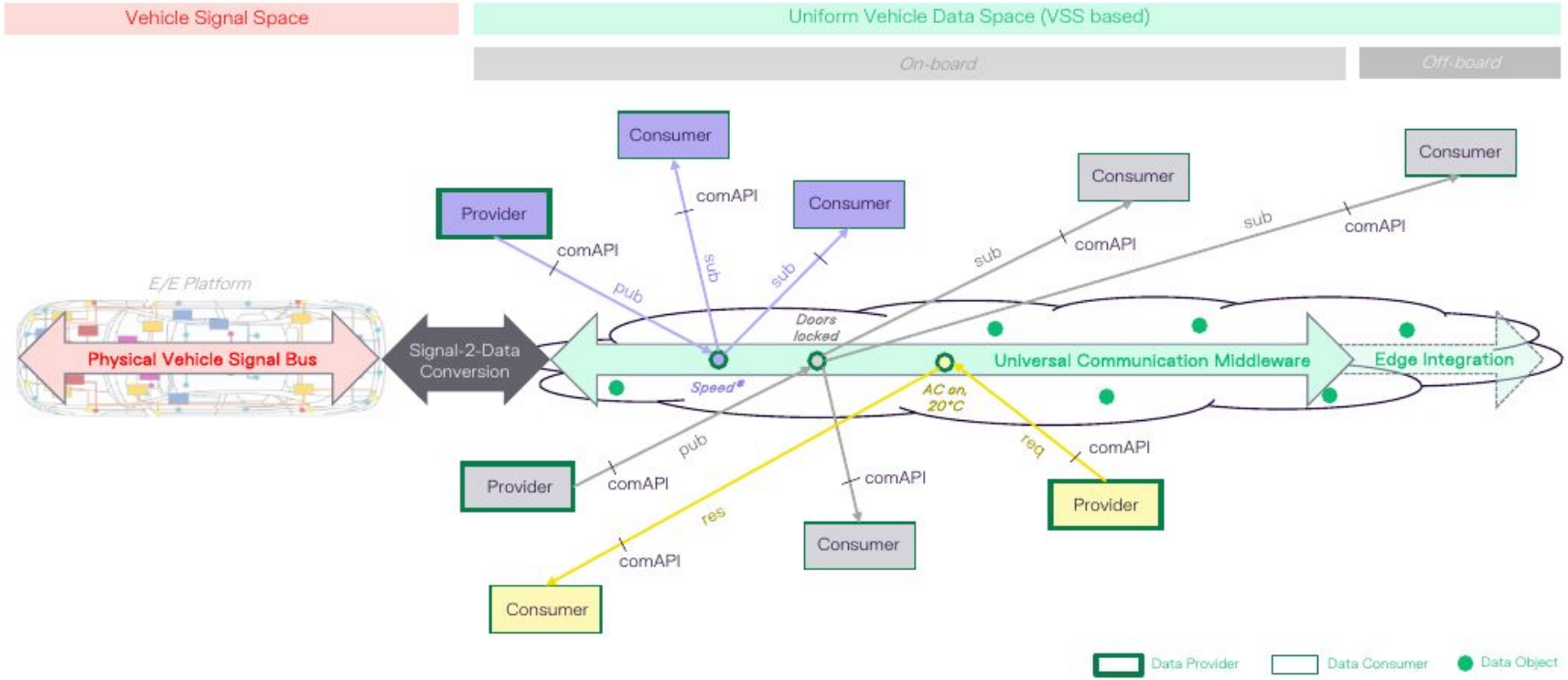
MLE provides an FPGA-based Rapid Prototyping System (RPS) catering to the specific needs of automotive engineers designing next-generation Zone Based Architectures.

MLE Auto/RPS enables automotive system engineers to design and to validate software-defined vehicle (SDV) functions along with MLE Auto/TSN in-vehicle networking.

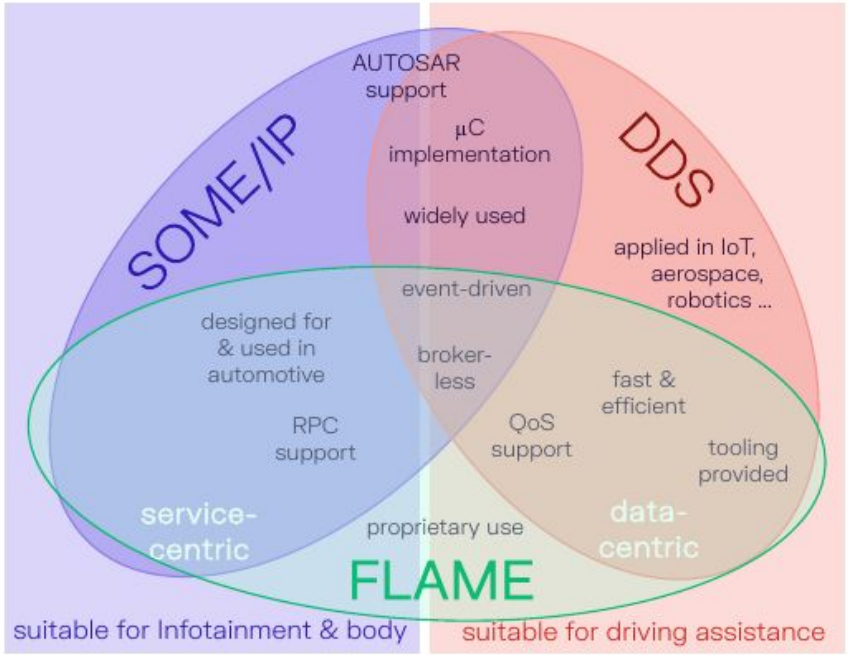
MLE Auto/RPS was designed as a shortcut into A-sample hardware development of Zonal Gateways / ECUs and implements an FPGA Full System Stack based on the Trenz Electronic TE0950-02 SoC-FPGA Development Kit featuring the AMD Versal AI Edge FPGA, and an automotive FPGA subsystem from MLE.



A data-centric SW architecture concept for the SDV



FLAME communication protocol is a flexible and efficient solution of the VW-Group for automotive

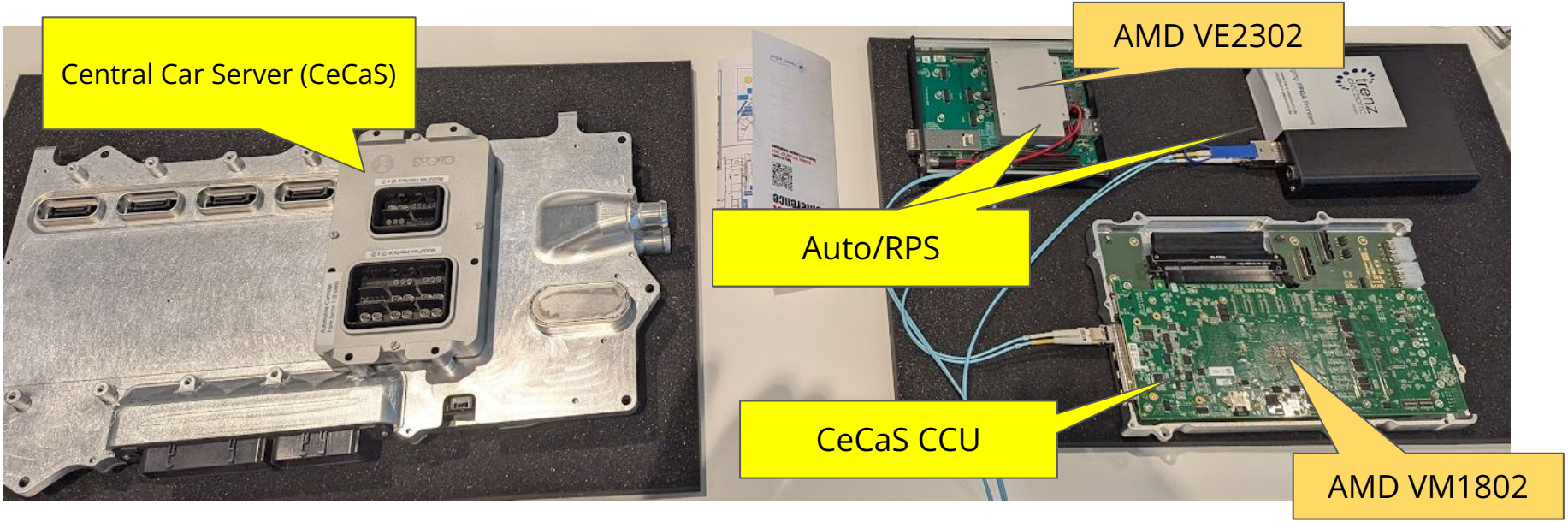


FLAME

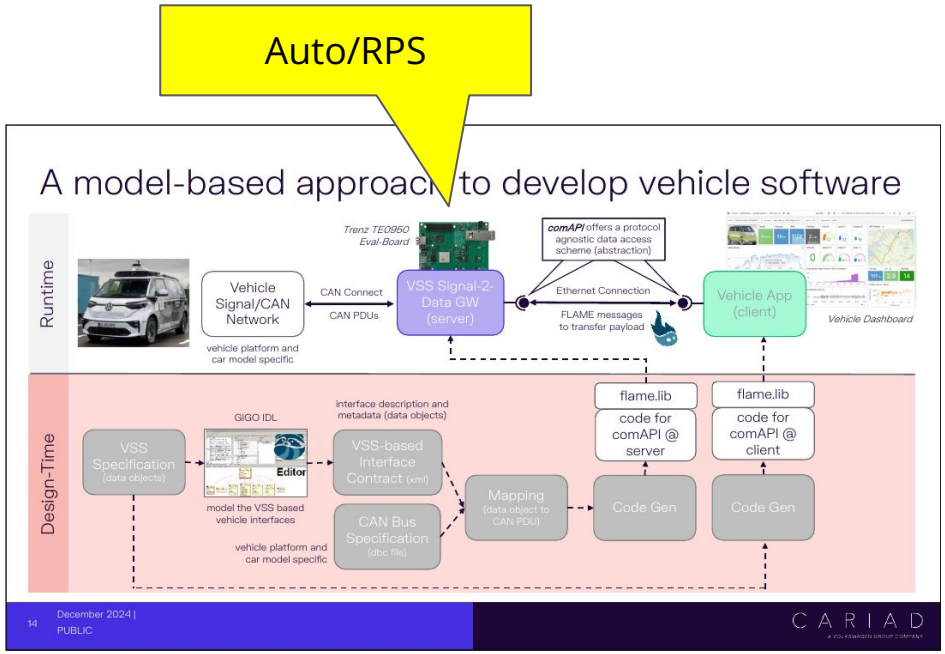
- FLAME (Flexible Automotive Middleware) is a middleware that combines service-oriented and data-centered communication
- Is was designed as a tailored automotive protocol to fulfill all the communication requirements across different domains in the vehicle
- It supports an RPC-mechanism (1 : 1 connection) to invoke remote functions by sending a request with parameters to a server-node, who replies with a respond message
- This is used for setting a configuration in a component, triggering a query or computation on a remote system node
- It also supports a publish-subscriber pattern (m : n connection) where consumers do not know the producer(s) and connection details
- This is for sending continuous/periodic state changes, the information is produced and published via topics (IDs)
- Easy-to-use tool (RACOON) for SW development & test which includes an IDL (GIGO) to formally describe data interfaces, assure the integrity of data-types and generation of code (server & client)

Auto/RPS in Action

Presented at BOSCH Automotive Ethernet Conference, Oct 2024, Renningen



Auto/RPS in Action



Auto/RPS in Action

Auto/RPS in Action: “LabCar” at VOLVO CampX

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