6G-ICAS4Mobility

Enabling PTP-based Time-of-Day Synchronization via 5G Sidelink

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MLE - Experts for Domain-Specific Compute Architectures

Our Mission: From Software to Silicon!

- Deliver HW and SW for High-Performance (Embedded) Compute Systems & Solutions
- Offering pre-validated subsystems with FPGA IP blocks and open-source software
- Support customer projects with deep expertise and hands-on design services

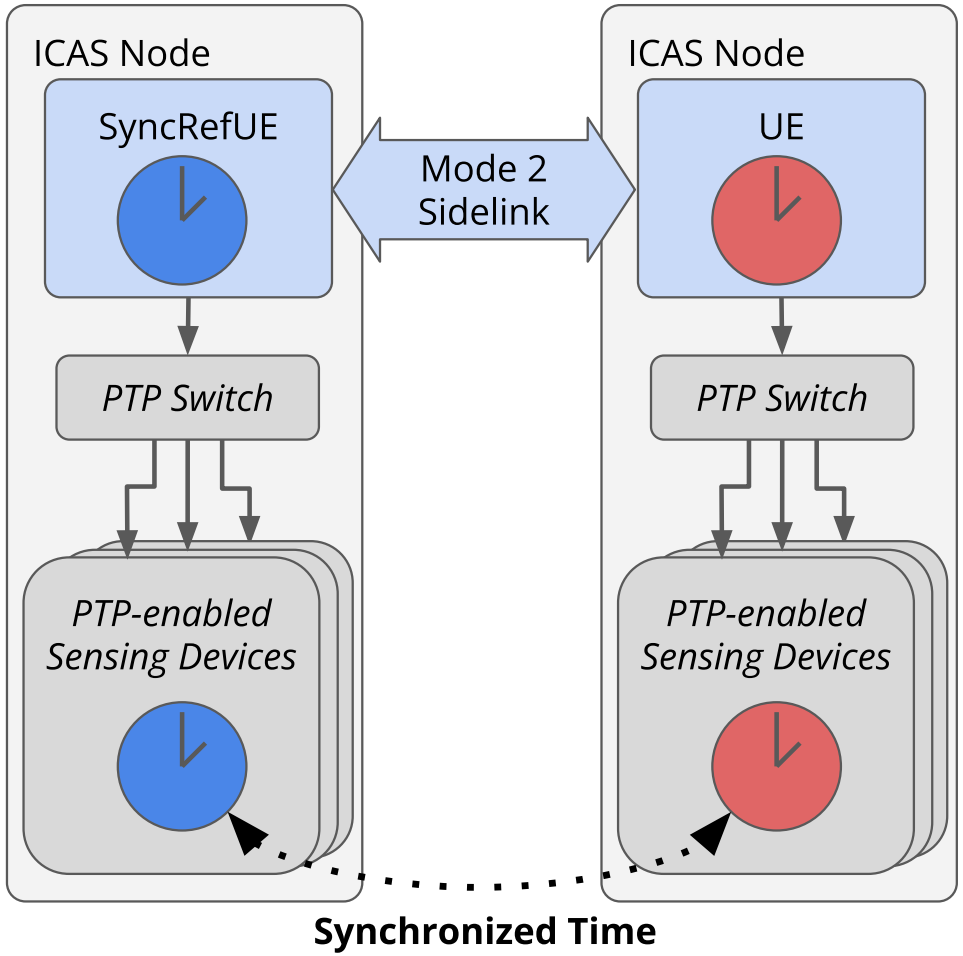
Headquartered in Silicon Valley with Design Offices in Germany

- Founded 2010, employee owned
- 20+ Certified FPGA Designers
- Customers include technology leaders, US and European government agencies, Fortune 500 companies
- Partners to:

Project Background: 6G-ICAS4Mobility

6G Integrated Communication and Sensing for Mobility

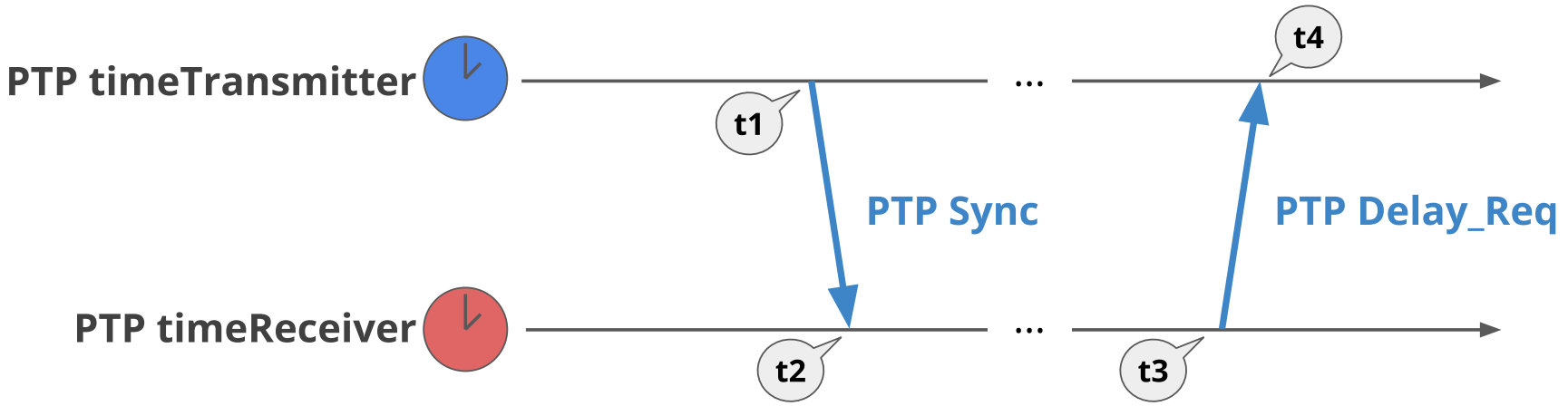
- **Sidelink-based ICAS** for mobile devices, use cases for vehicles and drones
- Contribution of MLE: **PTP-based application layer time synchronization over sidelink mode 2**
- Enables:
  - collaborative sensing
  - interference avoidance



PTP Synchronization Mechanism

Determining Clock Offset

$$\text{offset} = \frac{(t_2 - t_1) - (t_4 - t_3)}{2}$$



- **Determine offset of PTP timeReceiver clock from PTP timeTransmitter clock and adjust accordingly**
- Requires accurate TX/RX timestamps of PTP messages
- Timestamp *'beginning of the first symbol after the start of frame delimiter'* [IEEE1588-2018]
- **How to apply this to Sidelink communication?**

Summary of the Approach

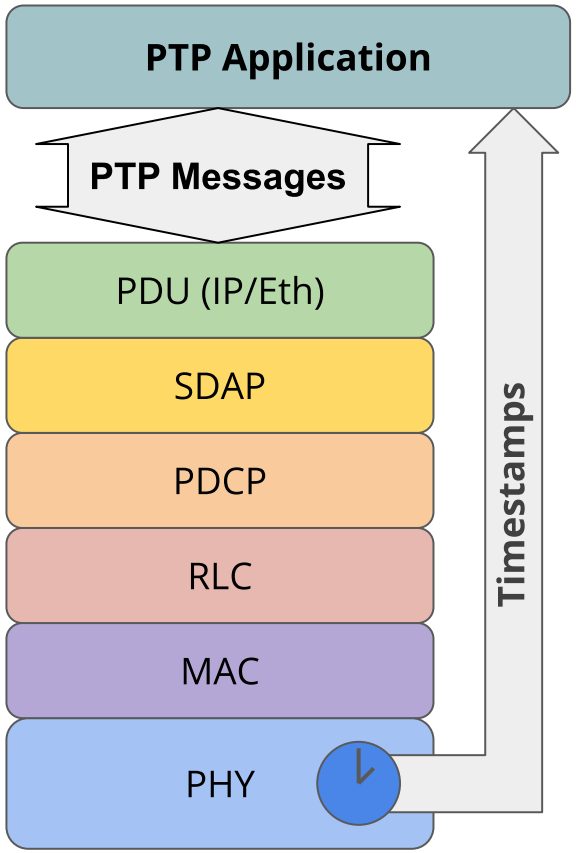
Steps towards PTP over Sidelink Mode 2

1. **Establish relationship between PTP Messages** in the Application Layer **and frame structure** of the PHY layer

   => Keep track of PTP messages through the protocol stack

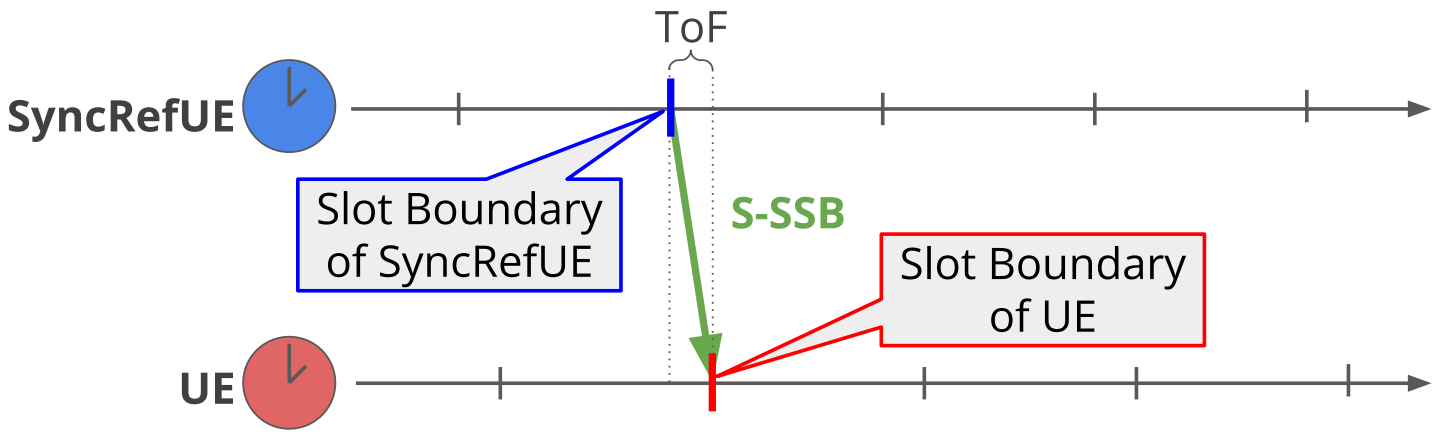
2. Choose appropriate timestamps in the PHY layer and assign them to the PTP packets on the application layer

   => Idea: Benefit from the existing PHY layer time domain synchronization



Time Domain Synchronization of the 5G NR PHY in Sidelink Mode 2

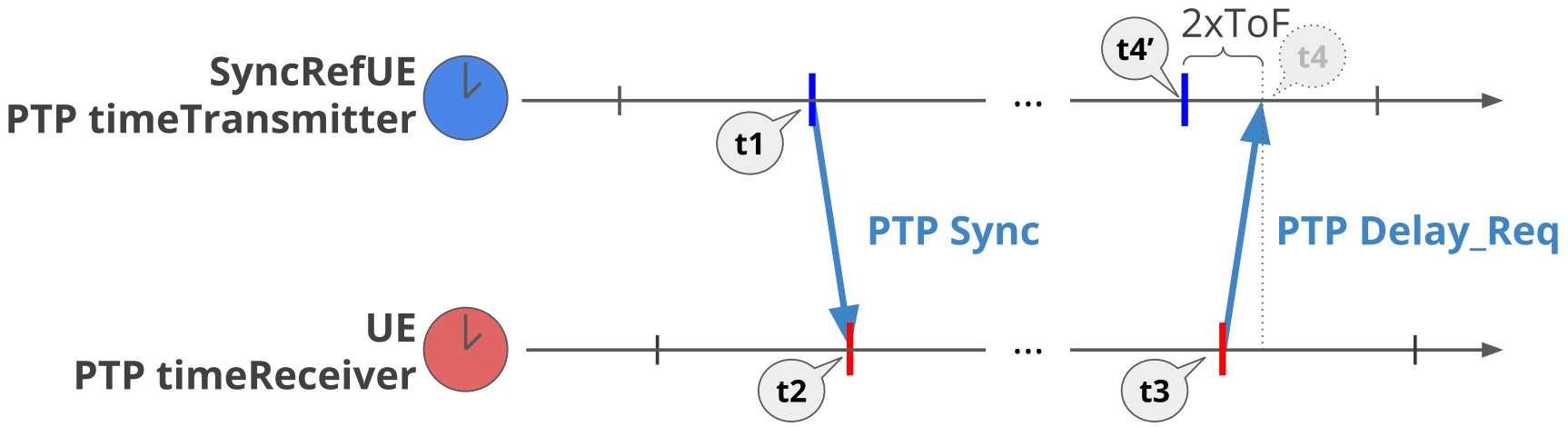
PHY layer already *is* synchronized in the time domain (frame/slot boundaries) – this is fundamental for the transmission of data!



=> Leverage the PHY synchronization: **use timestamps of slots containing PTP messages**

Integration of Timestamping for PTP

Using Slot Boundaries for Timestamps



✓ **t1, t3 (TX):** matches moment of physical transmission

✓ **t2 (RX at UE):** matches physical Time of Arrival (ToA) due to PHY layer sync

! **t4' (RX at SyncRefUE):** does not match physical ToA (t4), Error = 2*ToF

Implications of using Slot Timing for PTP Timestamps

- ToA error increases with distance by 2*ToF
- For the PTP offset calculation, this corresponds to an error = 1*ToF (assuming symmetric RTT)
- For low distances, the error is negligible when aiming for µs-level accuracy
- For ns-level accuracy, the ToA has to be determined...

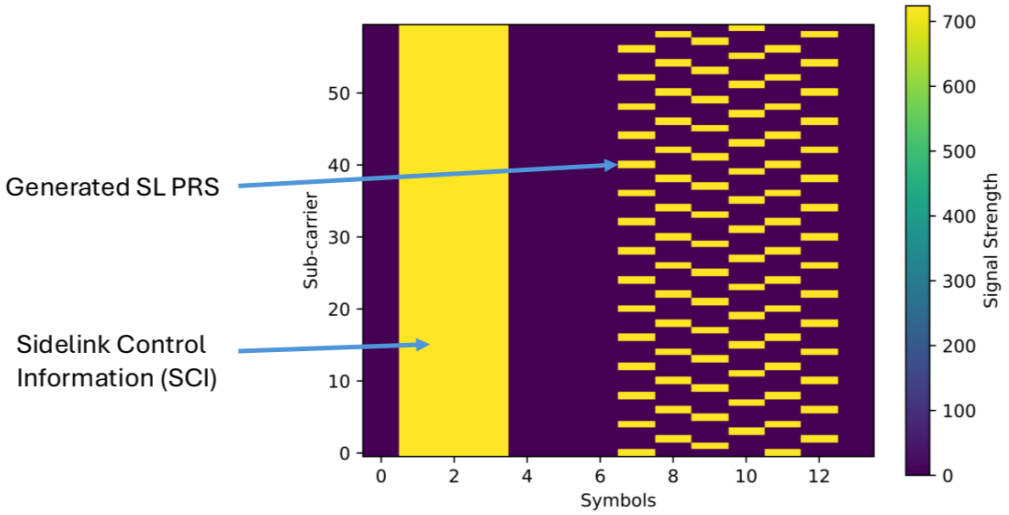
Distance	ToA Error = 2*ToF
1 m	6.671 ns
10 m	66.71 ns
100 m	667.1 ns
1000 m	6671 ns

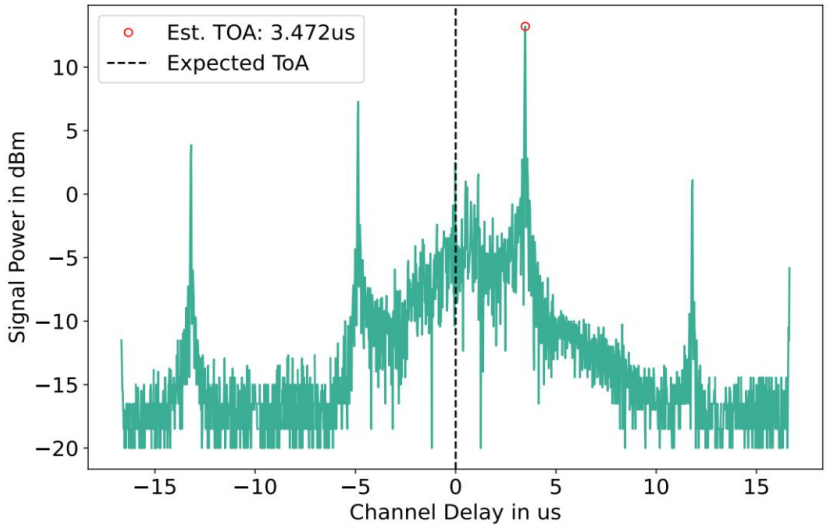
ToA Estimation using SL-PRS

Improving the Timestamping Accuracy

Fraunhofer HHI & mLe missing link electronics

- Determining ToA possible with pilot symbols, e.g. Sidelink Positioning Reference Signal (SL-PRS)
- Integration of SL-PRS to improve timestamp accuracy currently being researched by MLE and Fraunhofer HHI in a joint MA Thesis

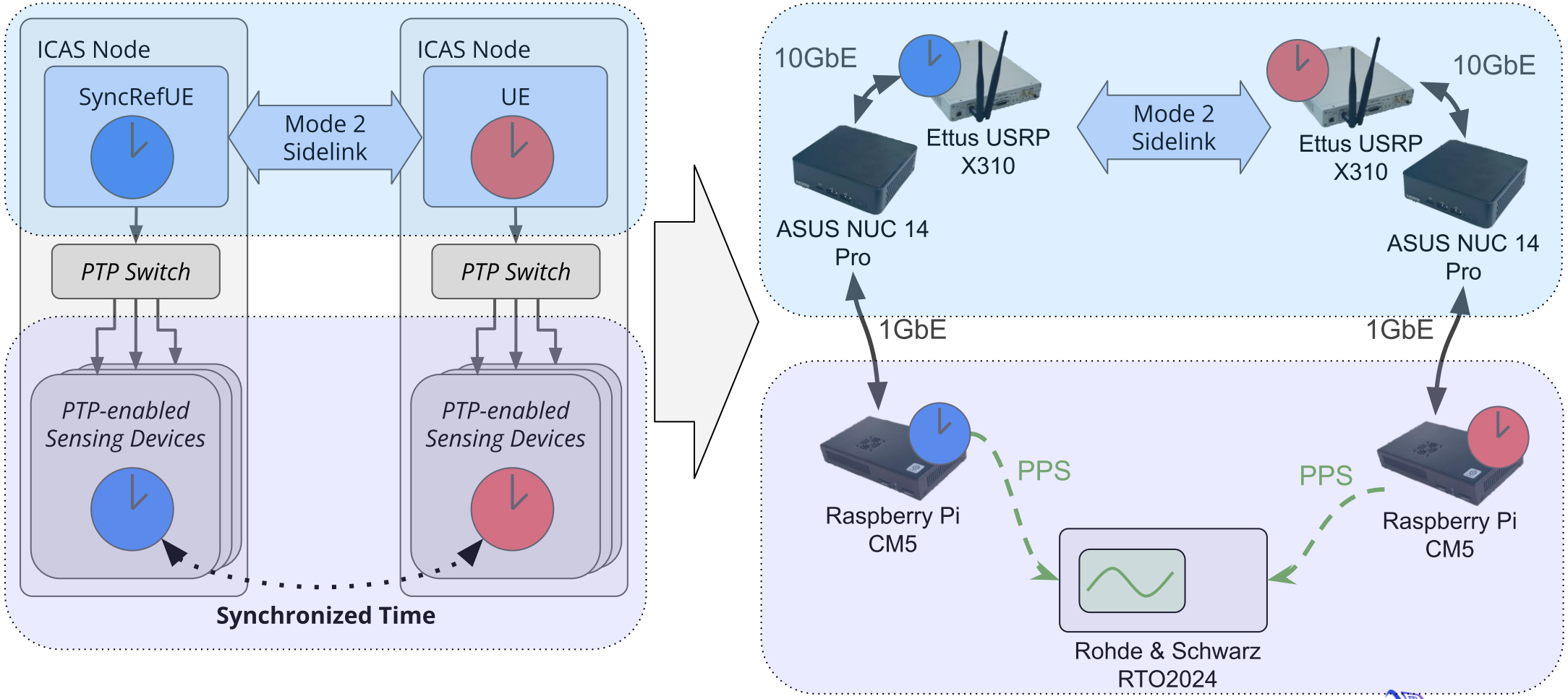




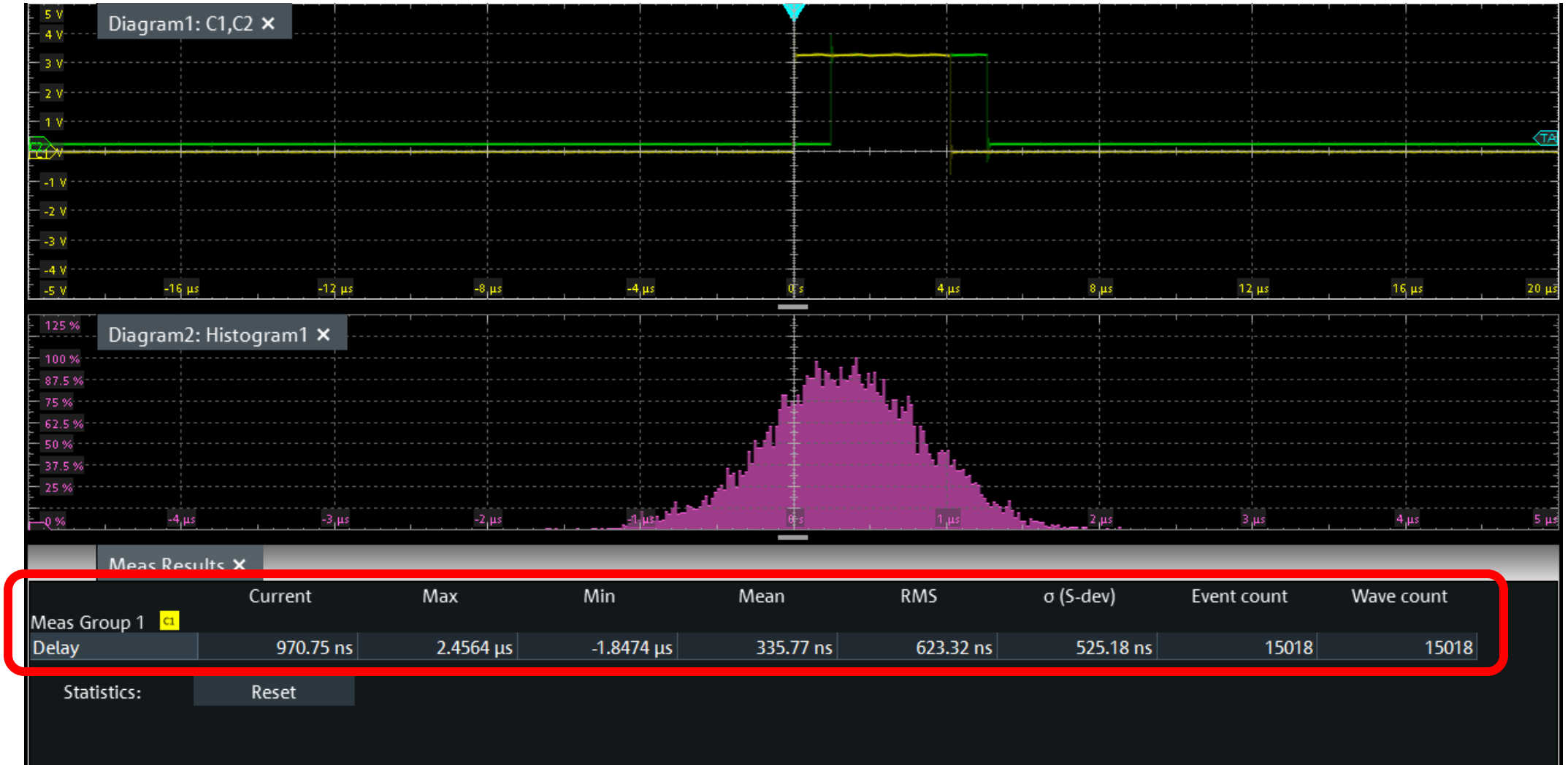
Demonstrator Setup

In Collaboration with Fraunhofer HHI

Fraunhofer HHI & mLe missing link electronics



Experimental Results



Summary and Implications for 6G

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- **Convenient, PTP-based time synchronization for applications**
- **µs-level time synchronization** achieved by deriving PTP timestamps from NR PHY slot timing
- ns-level synchronization requires precise ToA determination and optimized system architecture
- **No additions to 6G standard required:**
- Implementation relies on existing mechanisms and doesn't require changes to hardware...
- … but must be integrated with the PHY hardware clock and into Sidelink protocol stack