In-Vehicle Network - Automotive Zone Based Architecture with Time Sensitive Network

Maximilian Sokol
(Andreas Braun / Andreas Schuler)

About the Speaker

- **Friedrich Maximilian Sokol, M. Eng.**
  - "Full-Stack" Digital Hardware Engineer, Missing Link Electronics
  - Driving high-performance solutions from initial system architecture through to final hardware deployment.
- **Core Expertise: Protocols on Silicon**
  - Specialist in high-performance network stacks (TCP/IP) for FPGAs.
  - Expertise spans system architecture, PCB design, and low-level software.

MLE – Experts for Domain-Specific Compute Architectures

Our Mission: From Software to Silicon!

- Deliver HW and SW for High-Performance (Embedded) Compute Systems & Solutions
- Offering pre-validated subsystems with FPGA IP blocks and open-source software
- Support customer projects with deep expertise and hands-on design services

Head-quartered in Silicon Valley with Design Offices in Germany

- Founded 2010, employee owned
- 20+ Certified FPGA Designers
- Customers include technology leaders, US and European government agencies, Fortune 500 companies
- Partners to:

AMD Adaptive Computing Partner PREMIER

trenz electronic GmbH

PCI SIG

Fraunhofer IPMS

ulm university universität ulm

THU Technische Hochschule Ulm

ELEMASTER

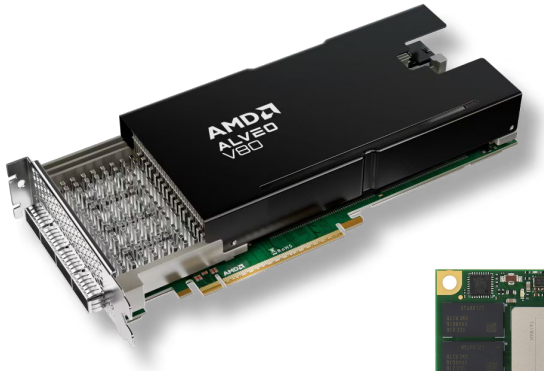
Fraunhofer Heinrich-Hertz-Institut

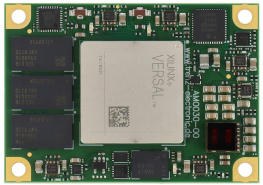
MLE Design Services Expertise – FPGA as a Computer

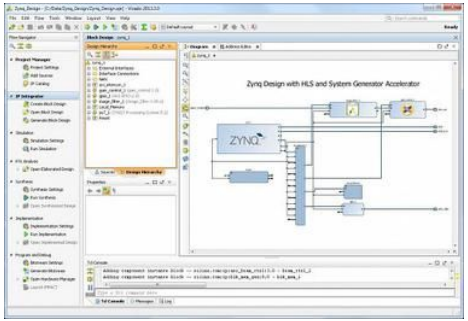
- RTL and High-Level Synthesis using FPGA design flows

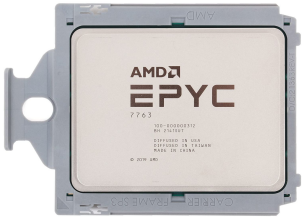
- AMD Zynq-7000 SoC in designs since Q1/2012
- AMD Zynq Ultrascale+ MPSoC in designs since Q4/2015
- AMD Zynq UltraScale+ RFSoC in designs since Q2/2018
- AMD Versal since Q1/2019
- PetaLinux / Vanilla Linux and Yocto-based SW development

- Multigigabit transceiver configurations
  - PCIe Gen2/3/4/5, SATA 3/6G, SAS 6/12G, NVMe, CXL
  - SDI-3/6/12G, JESD204B, DP/HDMI 4k, MIPI CSI-2 D-PHY
  - 10/25/40/50/100G Ethernet, Low Latency Ethernet
- Radar & Lidar for civil, mil/aero, automotive, industrial
- Image processing for HDMI, Displayport, SDI
- Time Sensitive Networking, Detnet, Layer-2/3 Switching
- Functional Safety Design Flows ISO 26262 (ASIL), IEC 61508 (SIL)
- Security & Trust (PUF, Crypto Accelerators , eFuses)







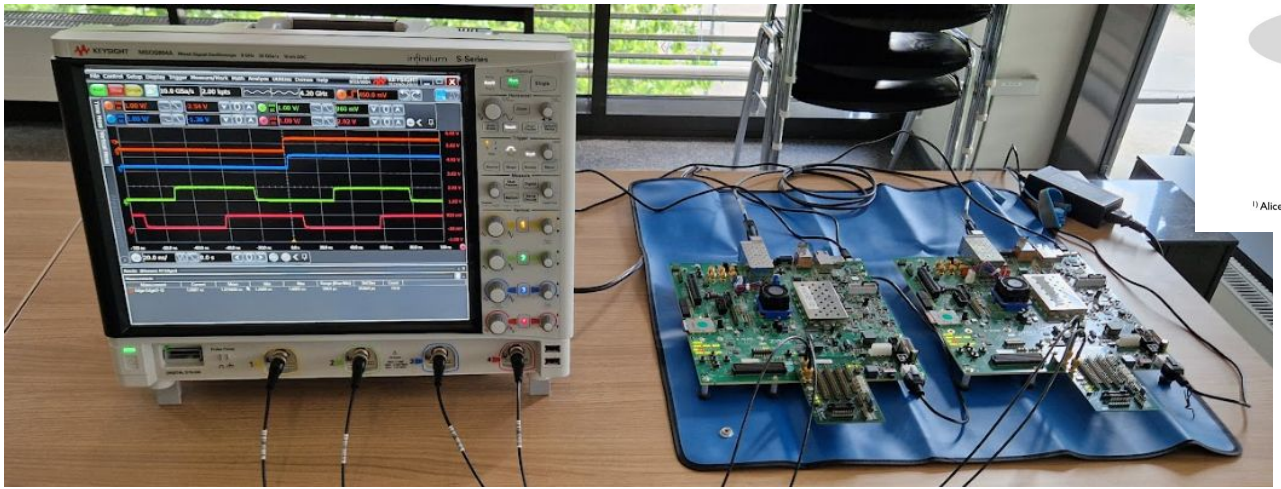


Our Technology Achievements

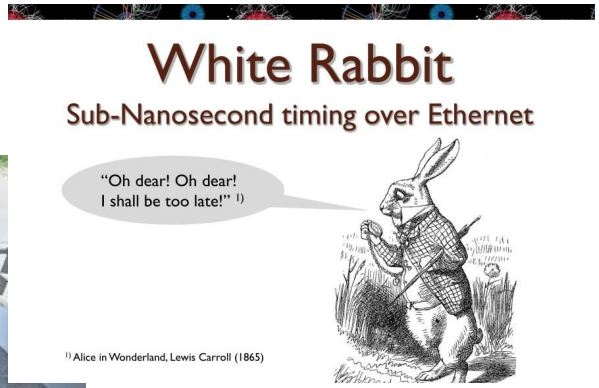
- Patented technology in the fields of acceleration, mixed-signal, functional safety
  - US Patent 9,209,828 – Configurable Mixed-Signal Systems
  - US Patent 10,140,049 – Partitioning Systems Operation in Multiple Domains
  - US Patent 10,509,880 – Automation for Configurable Mixed-Signal Systems
  - US Patent 10,708,199 – Heterogeneous Packet-Based Transport
  - US Patent 10,848,442 – Secure Heterogeneous Packet-Based Transport
  - US Patent 11,356,388 – Real-Time Multi-Protocol Heterogeneous Packet-Based Transport
- 60+ Presentations at Technology Conferences and in Technology Journals
  - Embedded World Conferences
  - PCI-SIG Developers Conferences
  - Flash Memory Summits, SmartNICs Summit
  - FPGA Conferences
  - IBM Open Power Summit
  - Automotive Ethernet Congress
  - XILINX Developer Forum and Security Workshops
  - SNIA Storage Developers Conferences

MLE Technology - Proudly Sourced Elsewhere

Example BMBF VERANO: Koherent digital Radar

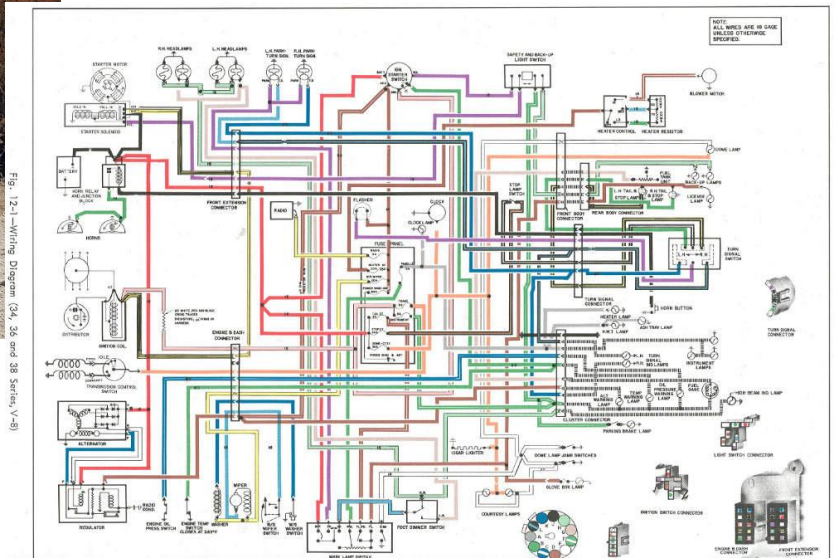


MLE optimizes CERN OHL White Rabbit to AMD/Xilinx FPGAs

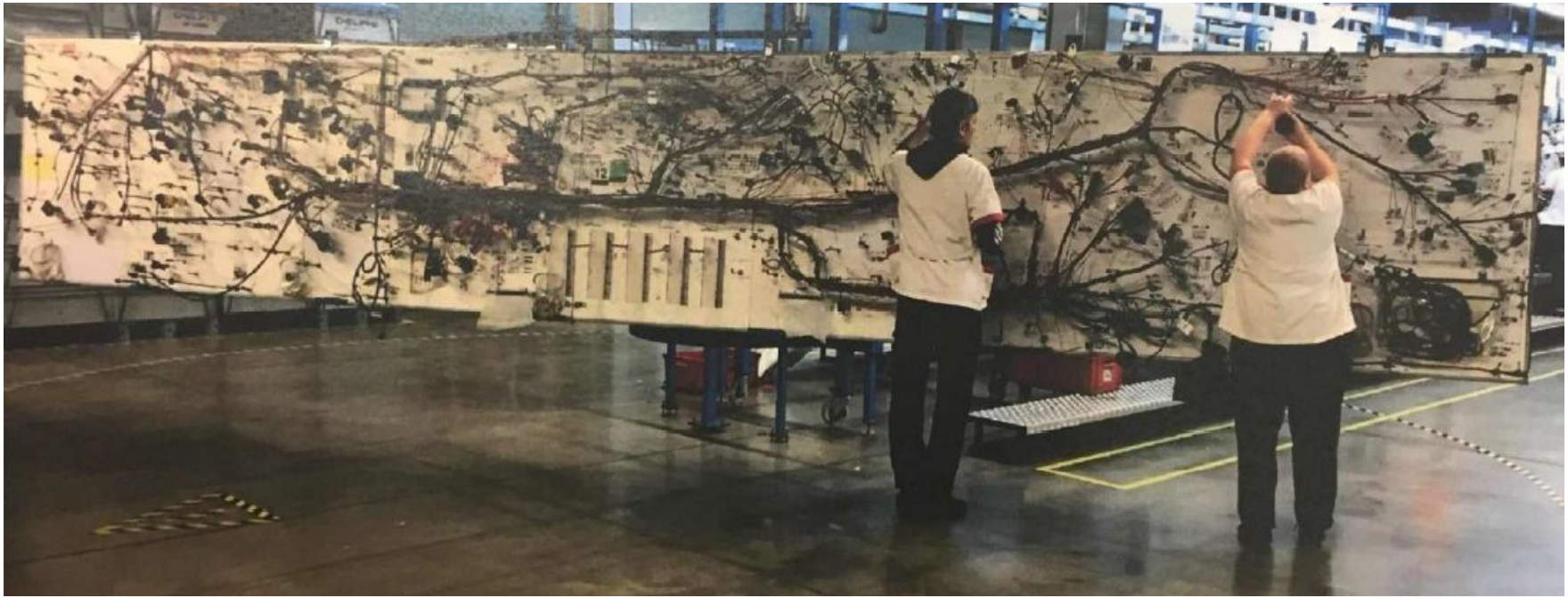


Automotive Network History (1967)

1966 Oldsmobile Cutlass Convertible

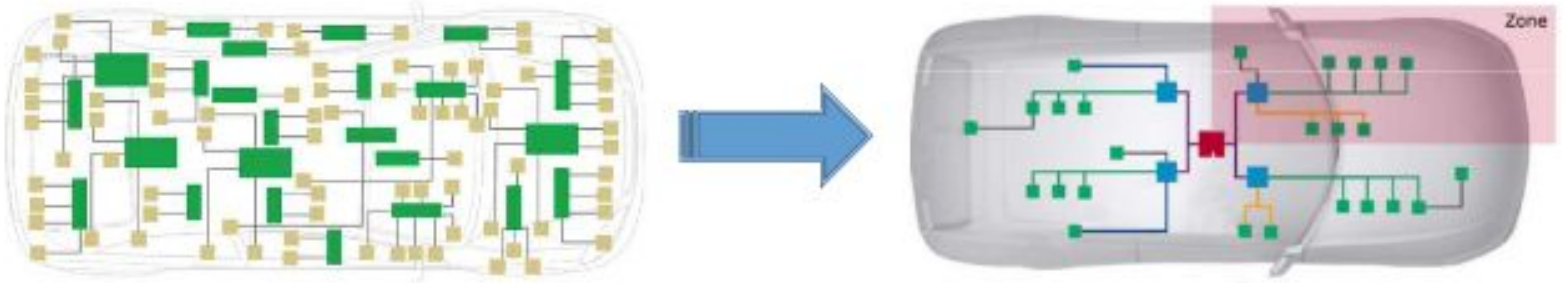


Today’s Expensive Wiring Nightmare



Next: Zone-Based Architectures

- Network connectivity is not based on functional domains, but on *physical location and proximity* inside the vehicle, i.e. “Zones”
- Data aggregation and preprocessing in Zone Controllers:
- High-bandwidth connectivity towards a central “High Performance Computer” HPC



Next: Zone-Based Architectures

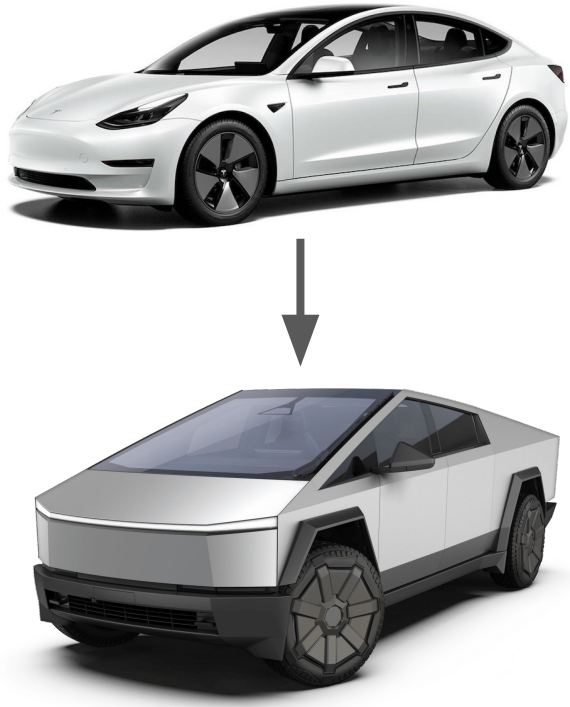
Example: **Tesla's “Etherloop”**[1]

Model 3:

- Number of endpoints: 273
- Number of cables: 490

Cybertruck:

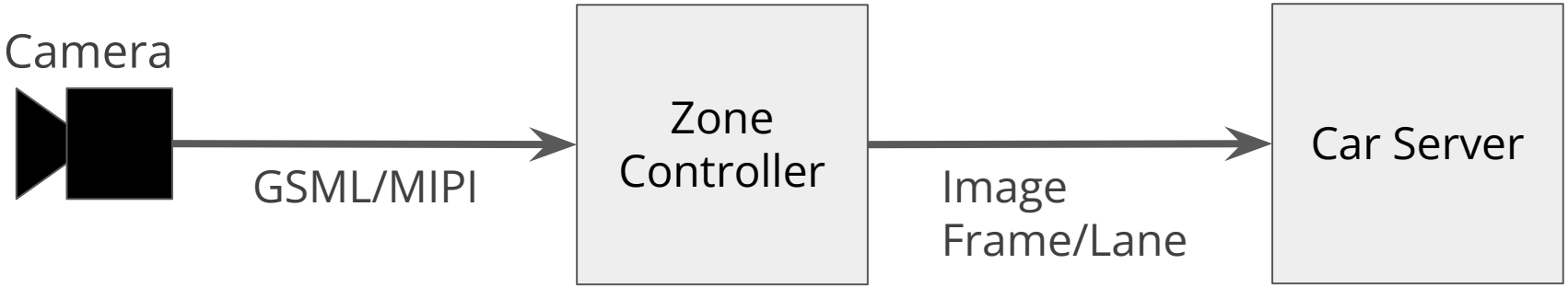
- Number of endpoints: 368
- Number of cables: 155



[1] https://insidetesla.de/tesla-cybertruck-innovatives-etherloop-system/

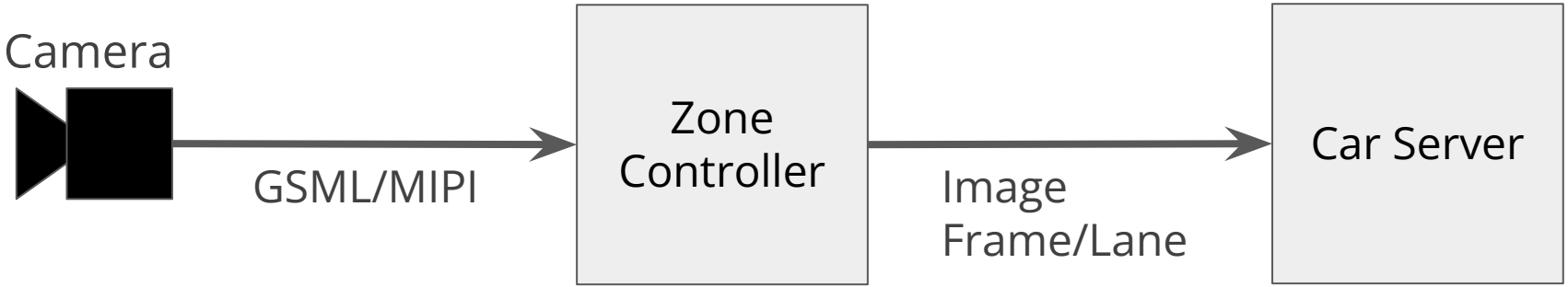
Why Zone Based Architecture? Signal 2 Data

Example: Camera



Why Zone Based Architecture? Signal 2 Data

Example: Camera

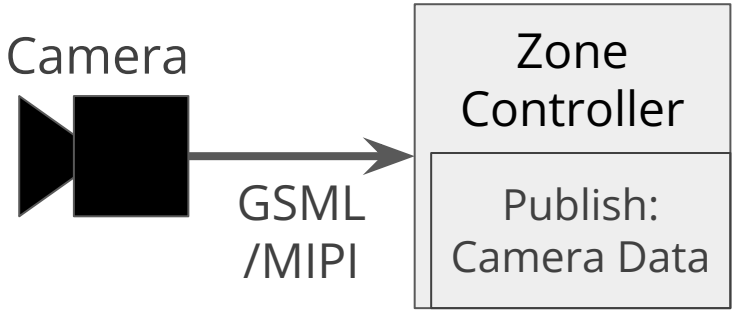


Zone can provide preprocessed data:

- Rescaled
- ROI
- etc.

Why Zone Based Architecture? Signal 2 Data

Middleware: pub / sub architecture



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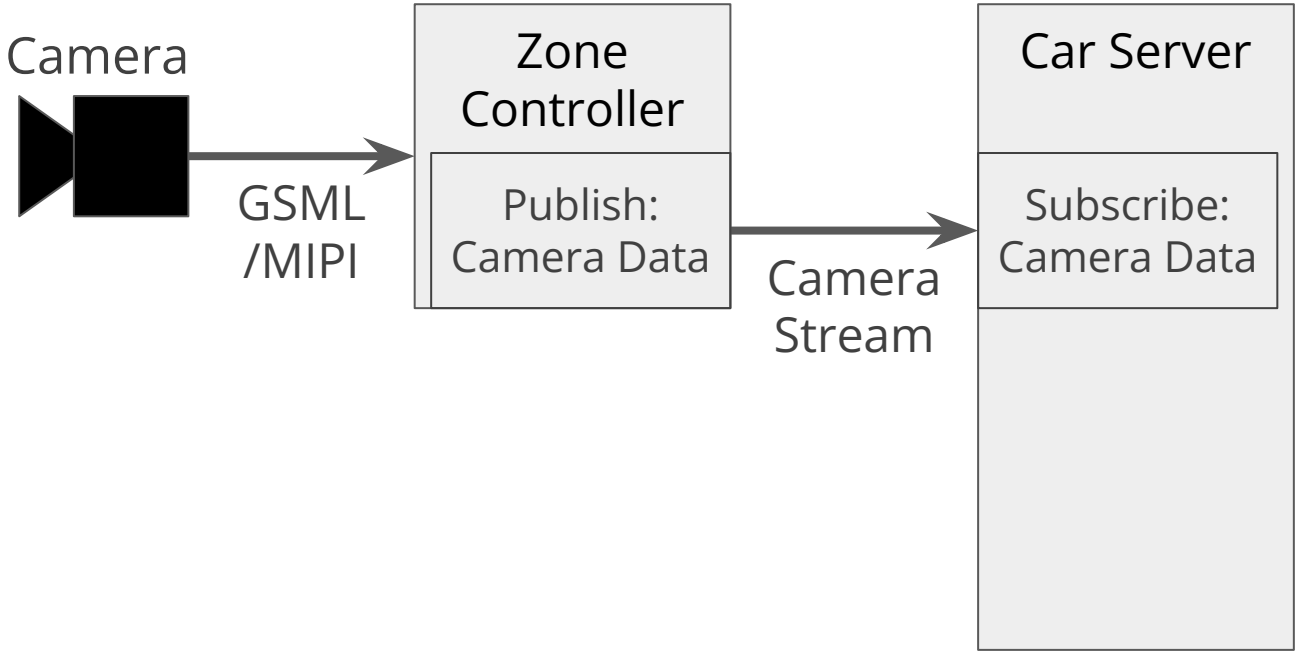

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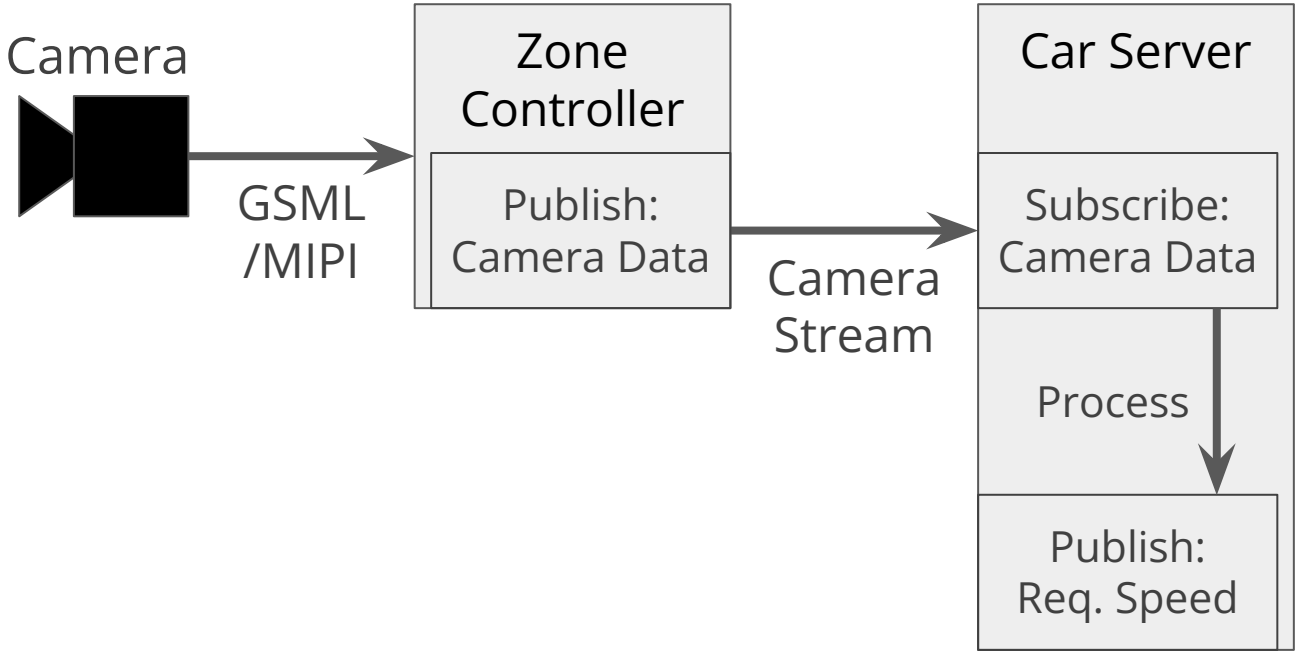

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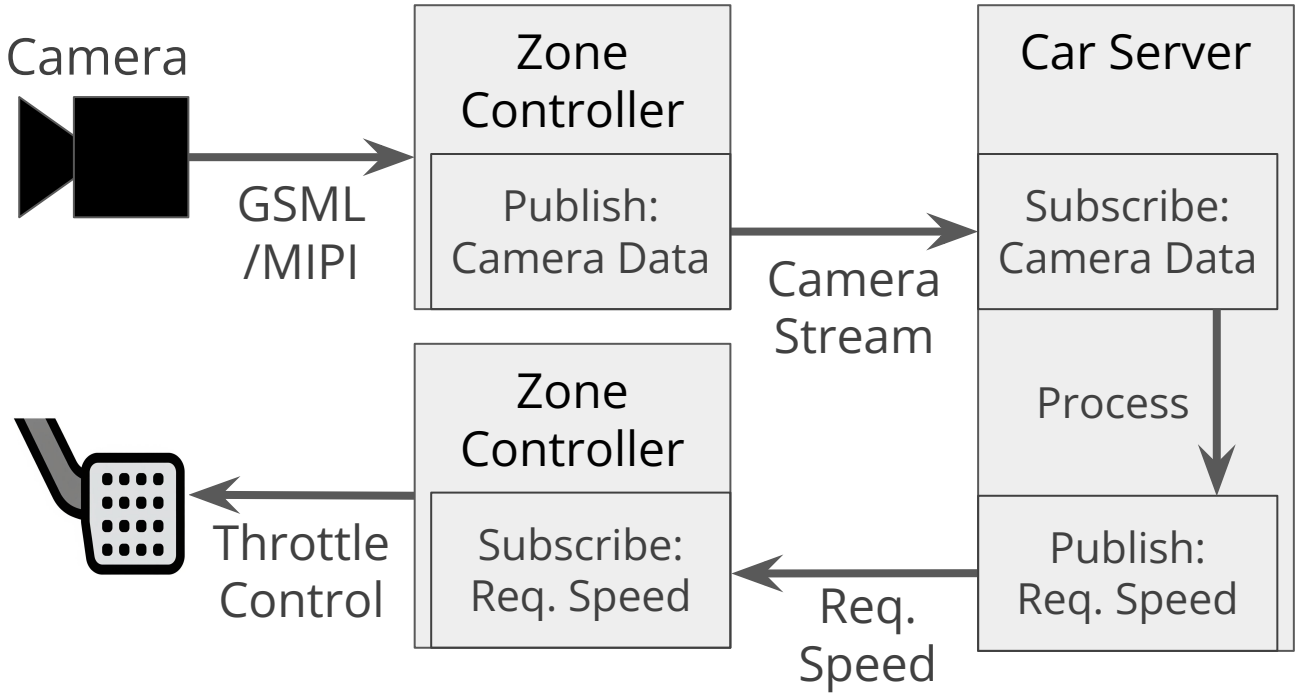

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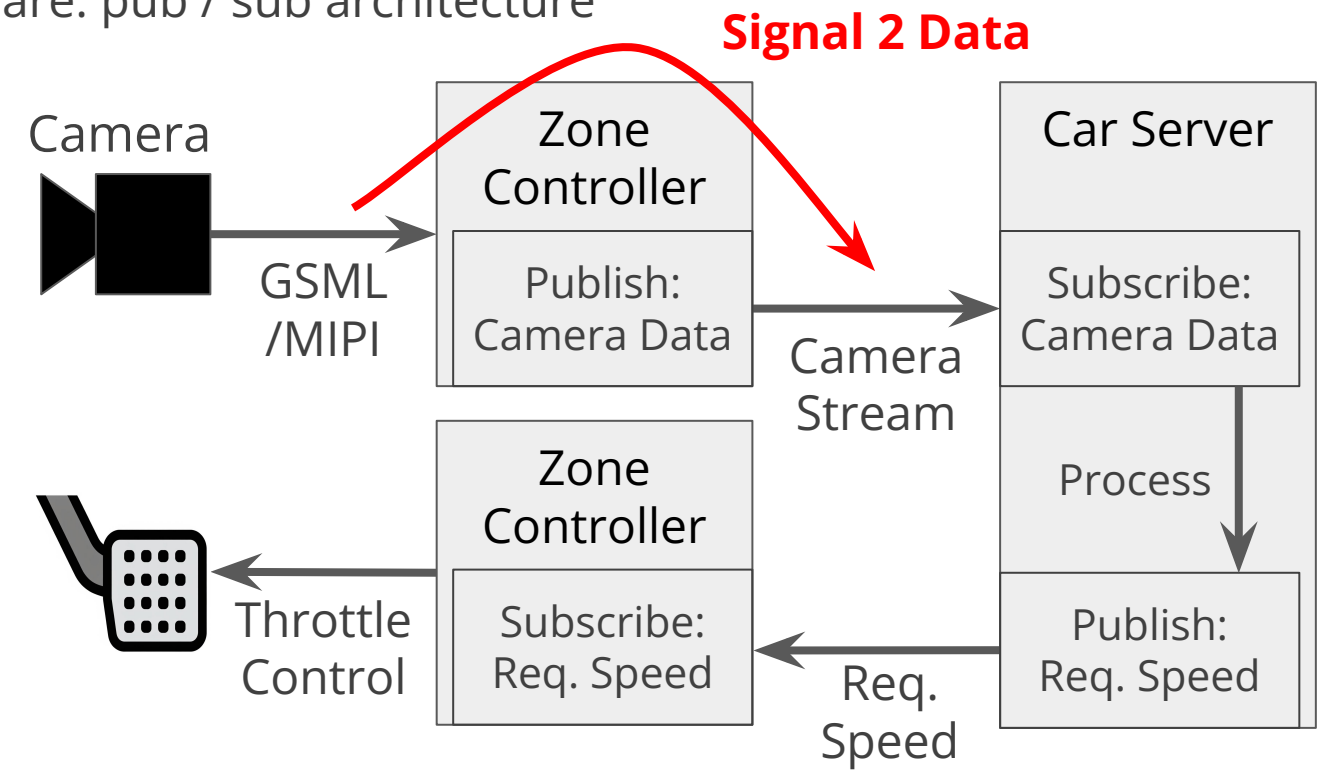

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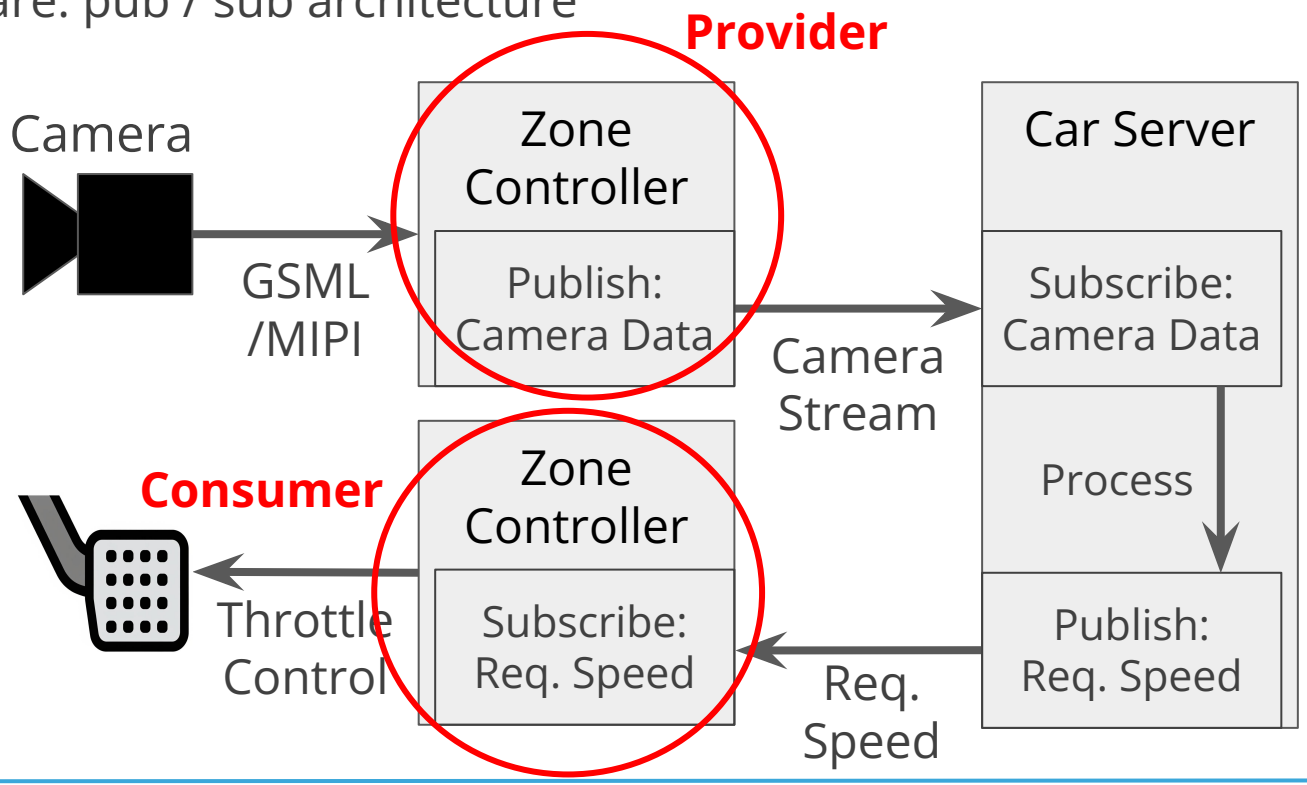
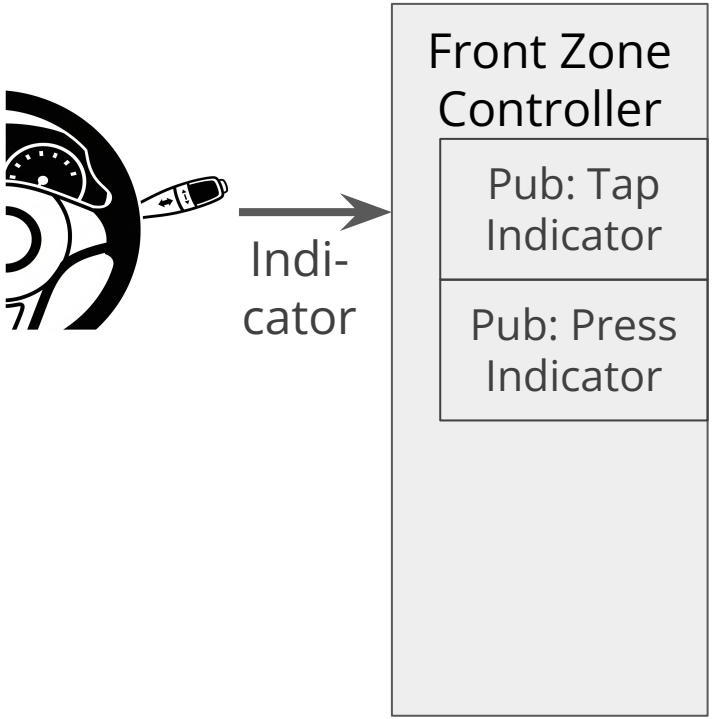


Why Zone Based Architecture? Signal 2 Data

Middleware: pub / sub architecture: Different example



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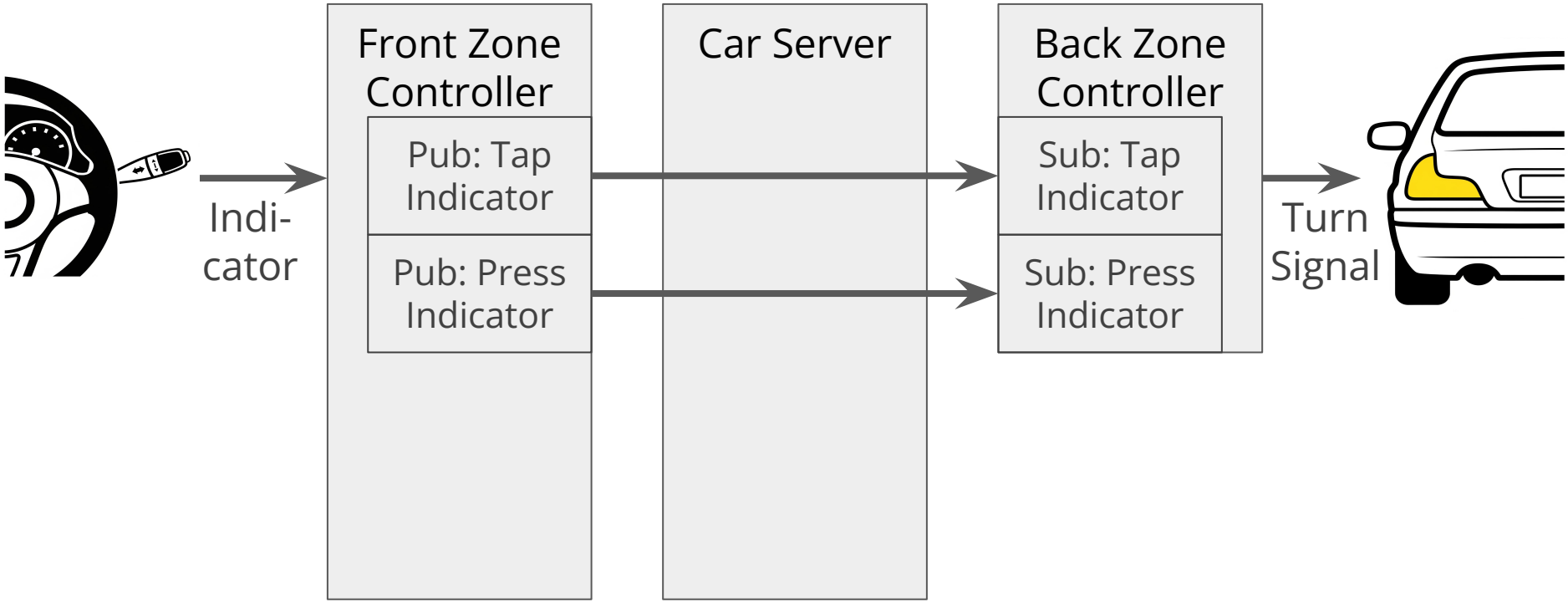

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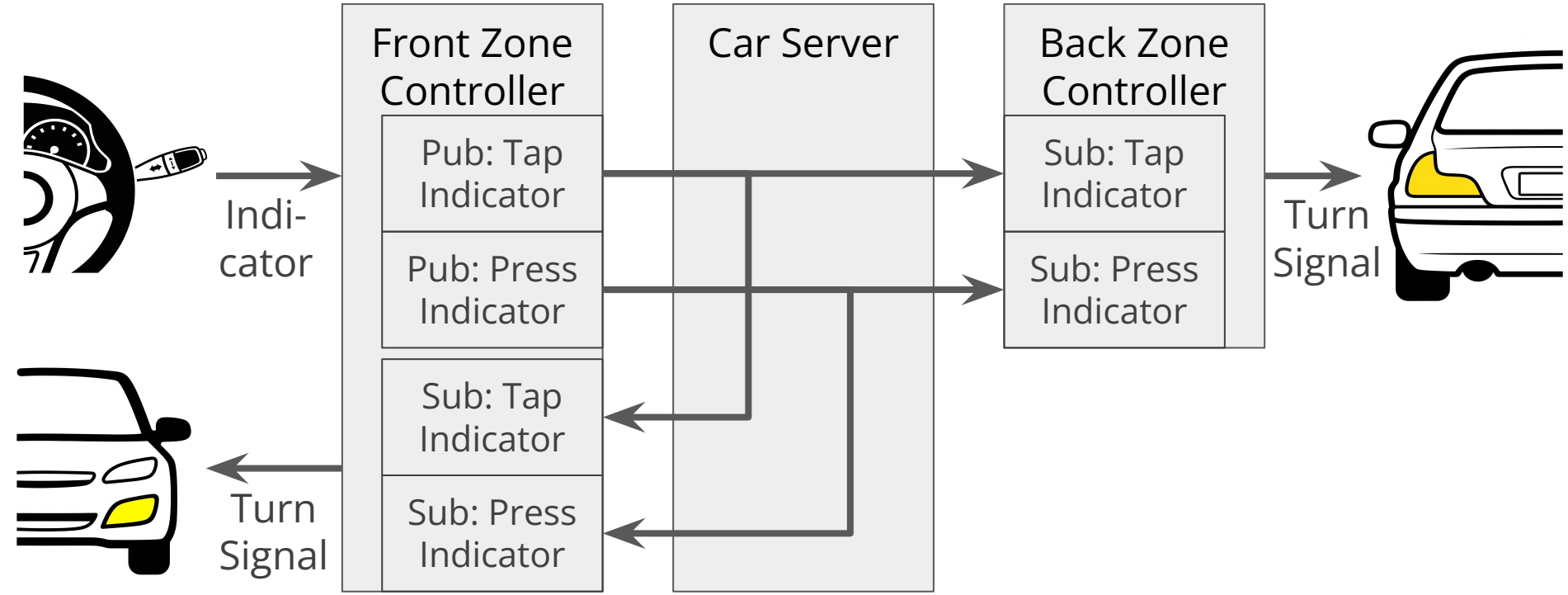

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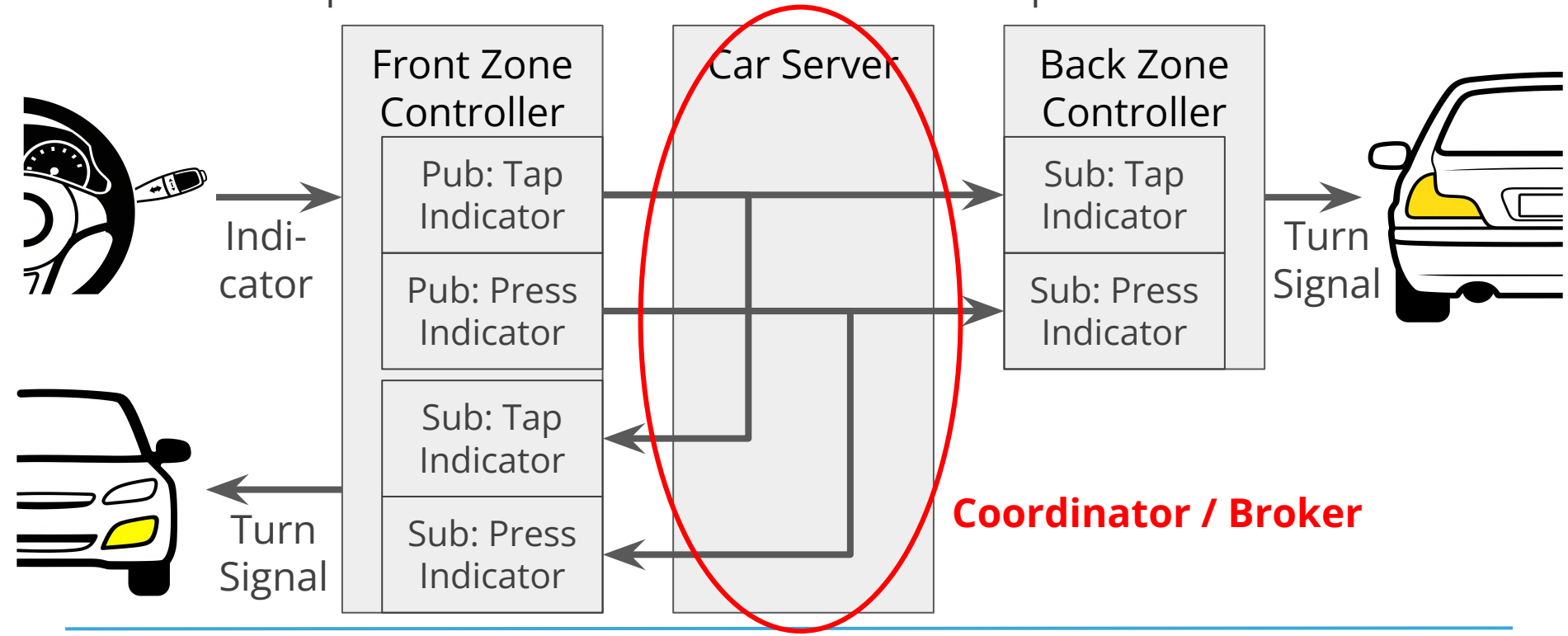

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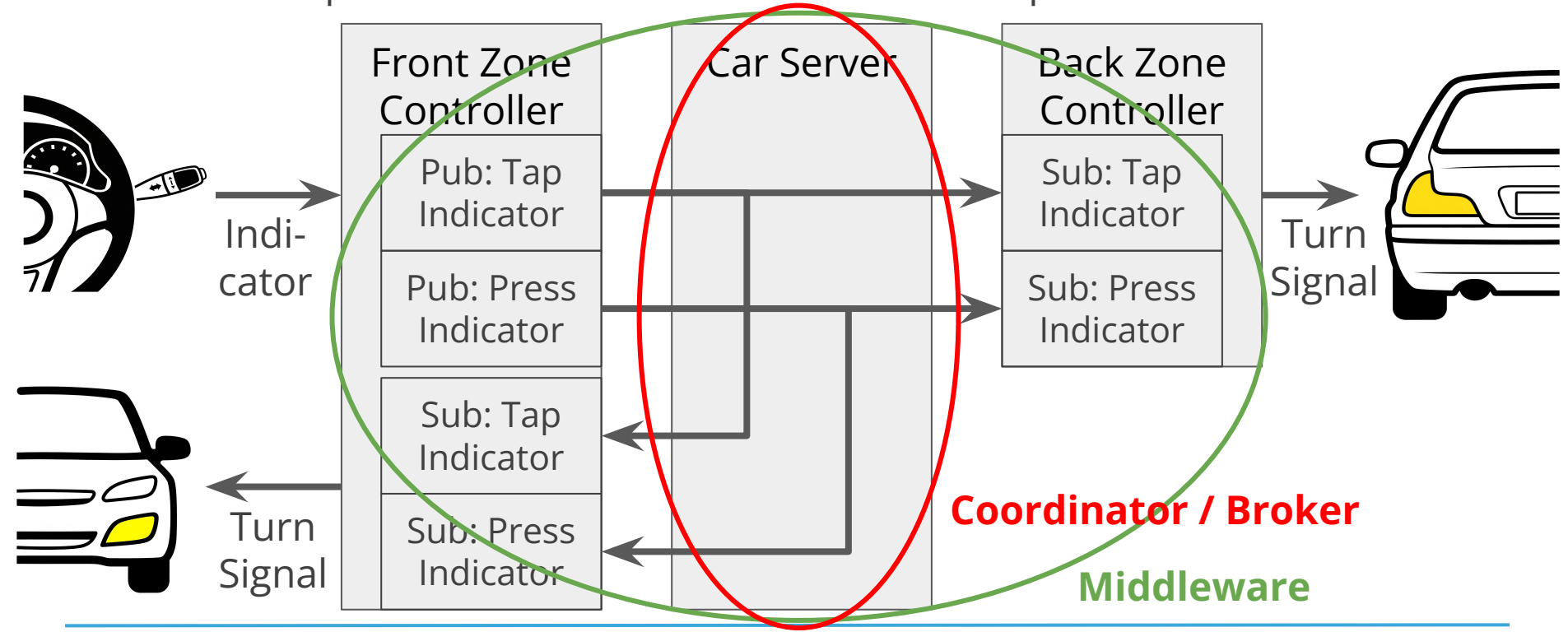

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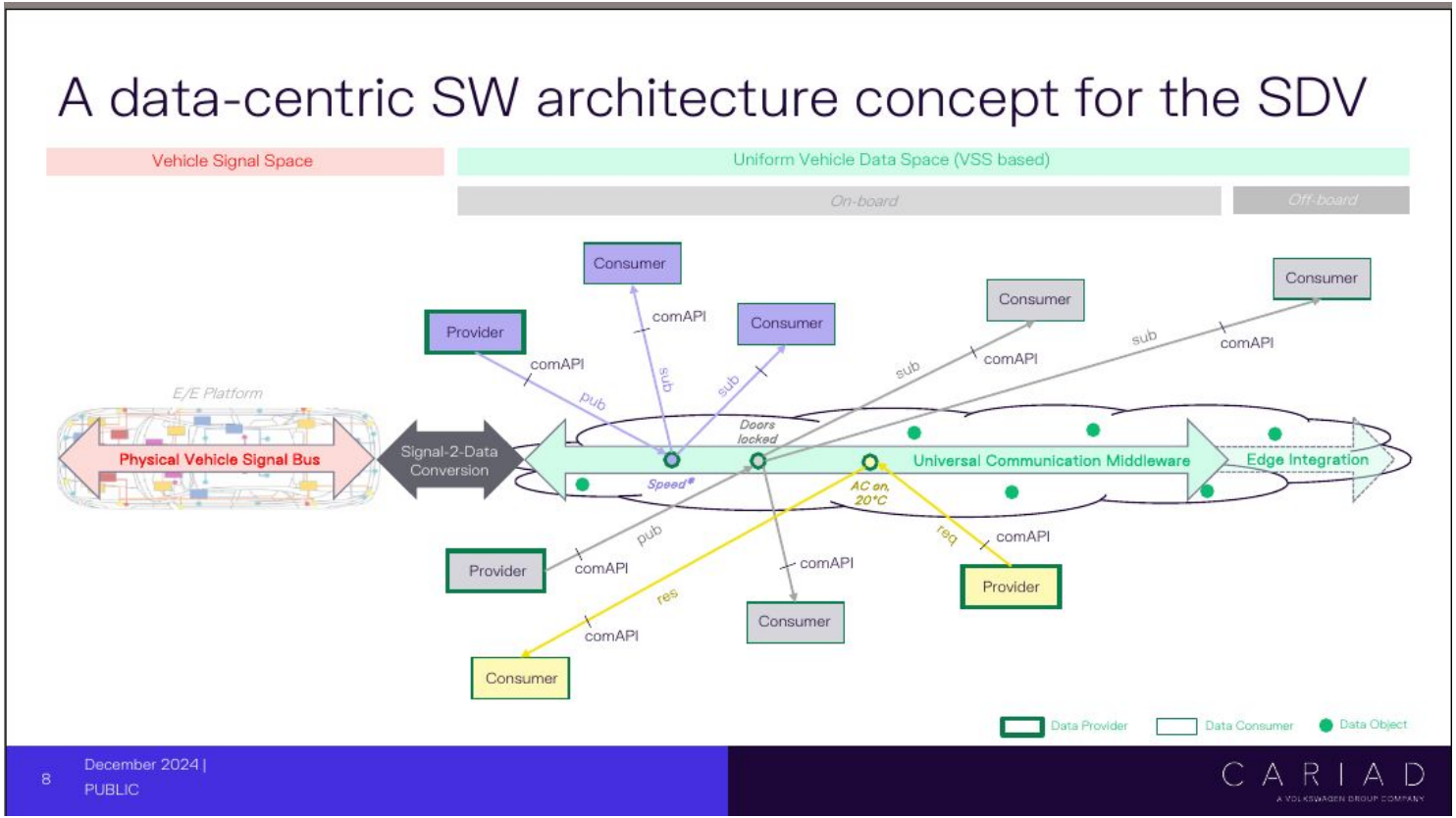
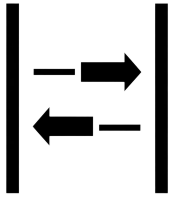


A Big Technological Challenge

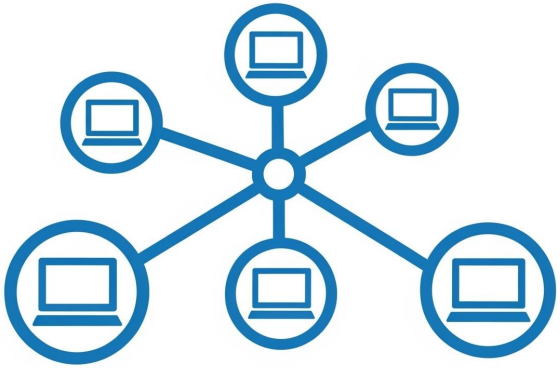
High Bandwidth



Low-Latency

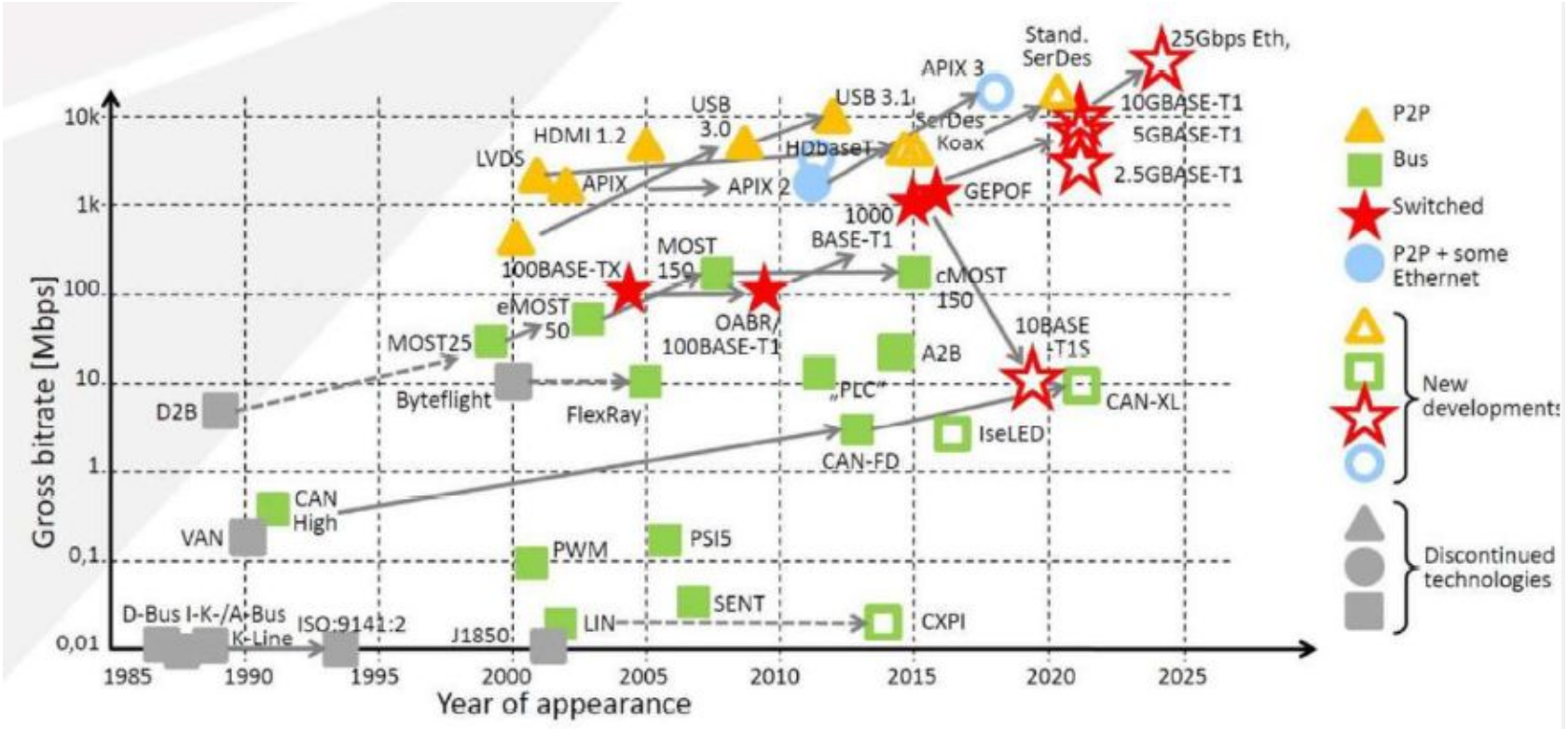
Reliable

Time-Deterministic



Networking

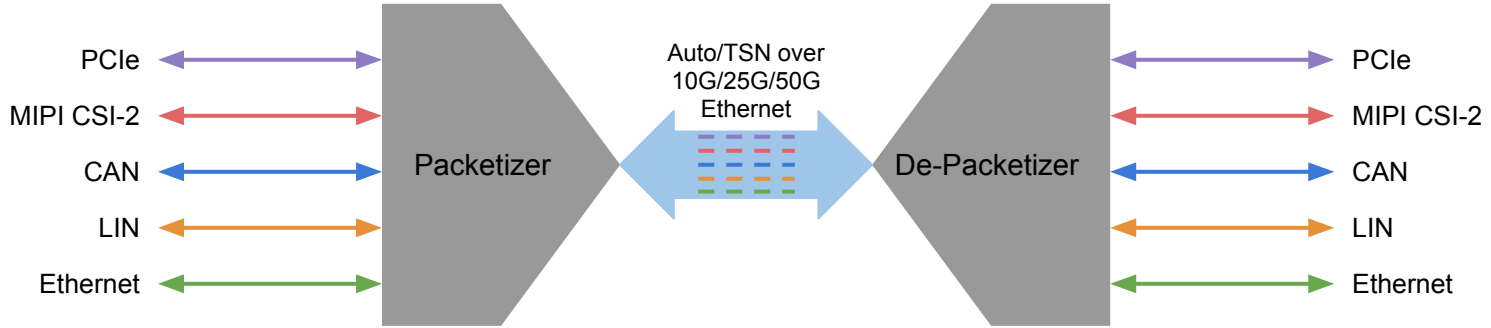
Evolution of Automotive Networks



Auto/TSN for Zone Architectures / in-vehicle network

Automotive data over Time-Sensitive Networks, based on open IEEE standards

- Virtualizes in-vehicle network infrastructure
- Full “legacy” connectivity plus enabling “new” high data rate interfaces (PCIe, GMSL, MIPI CSI2)
- Delivers bandwidth, scalability, security, Functional Safety



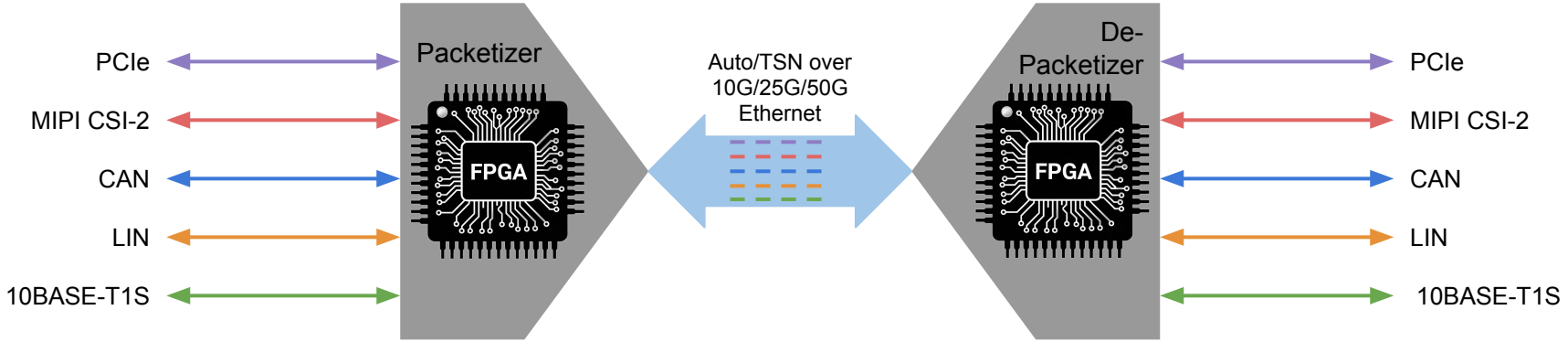
BOSCH

Multi-Gigabit Automotive Ethernet with AMD Kria KR260 Robotics FPGA Starter Kit

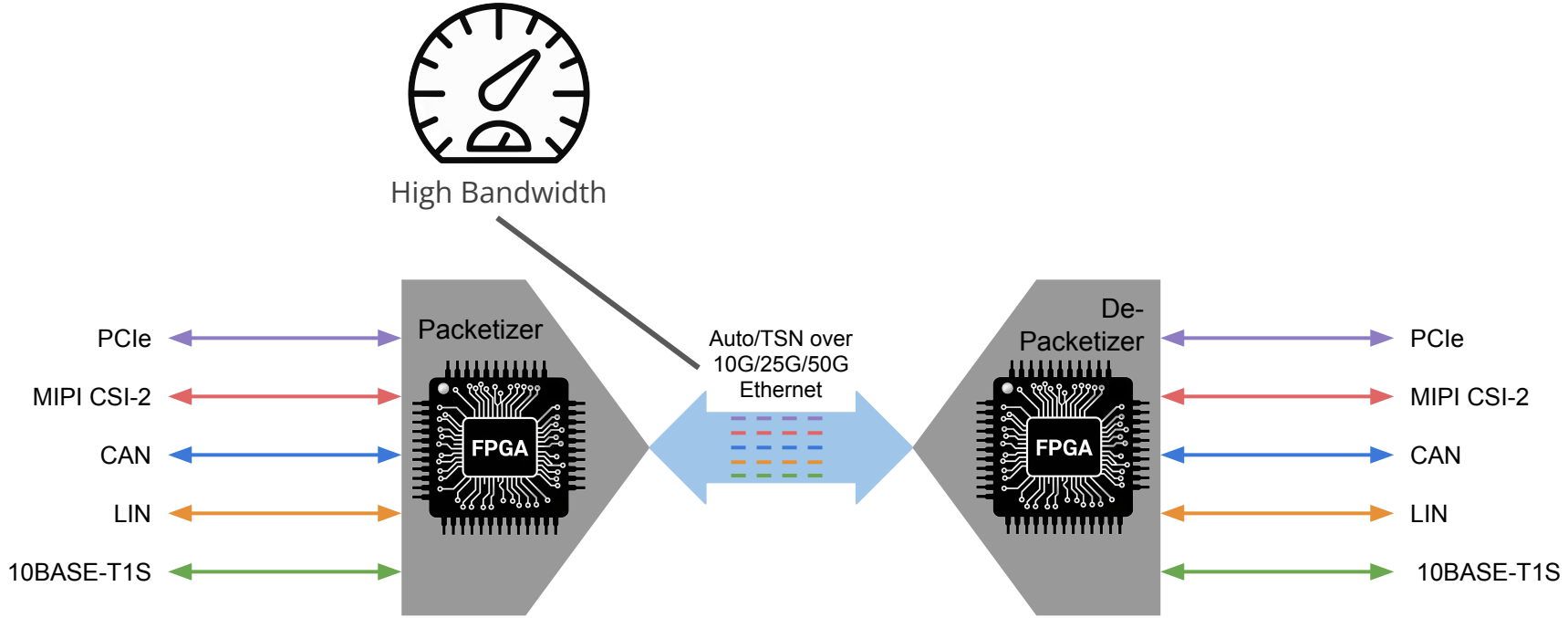
Nov 23, 2023 | 7 Months Ago

AMD's Kria KR260 Robotics Starter Kit builds on the success of AMD's Kria System-on-Modules (SoM) and is an ideal platform to test ideas for multi-Gigabit networking. Because Kria KR260 integrates...

Auto/TSN for Zone Architectures / in-vehicle network



Auto/TSN for Zone Architectures / in-vehicle network



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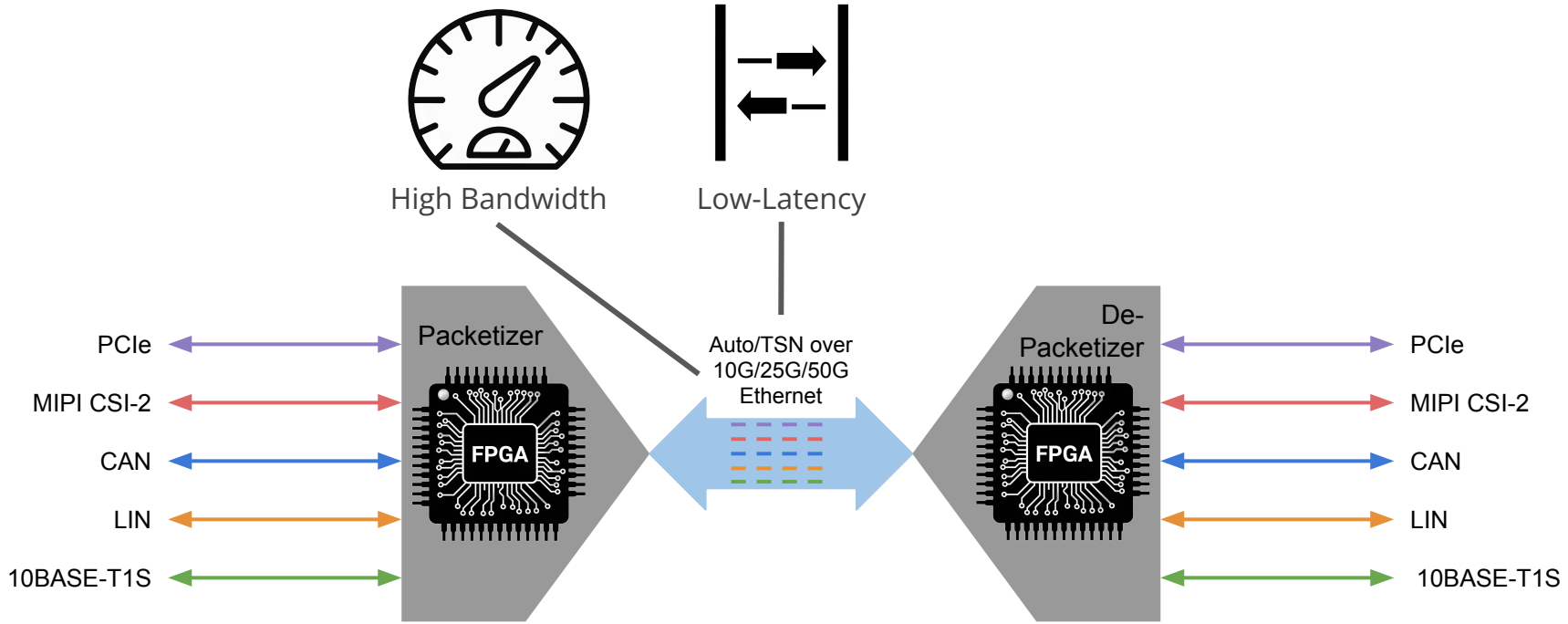

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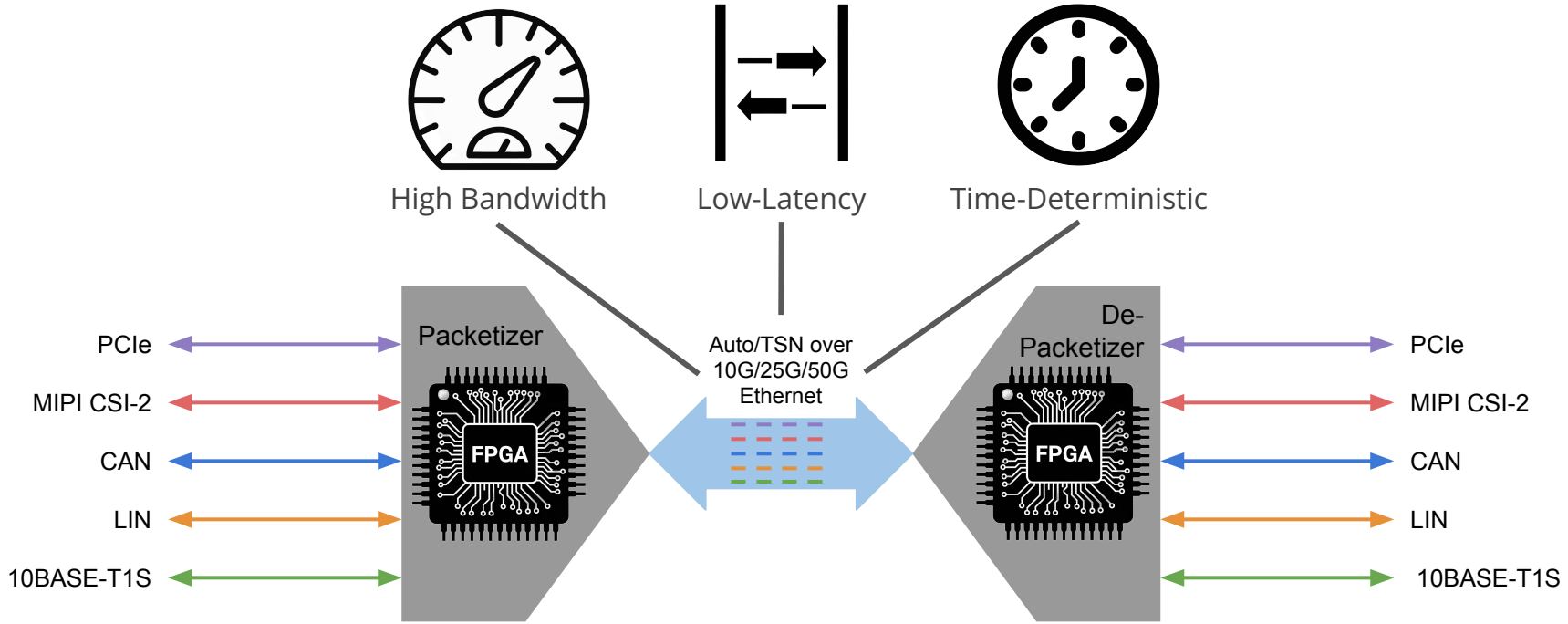

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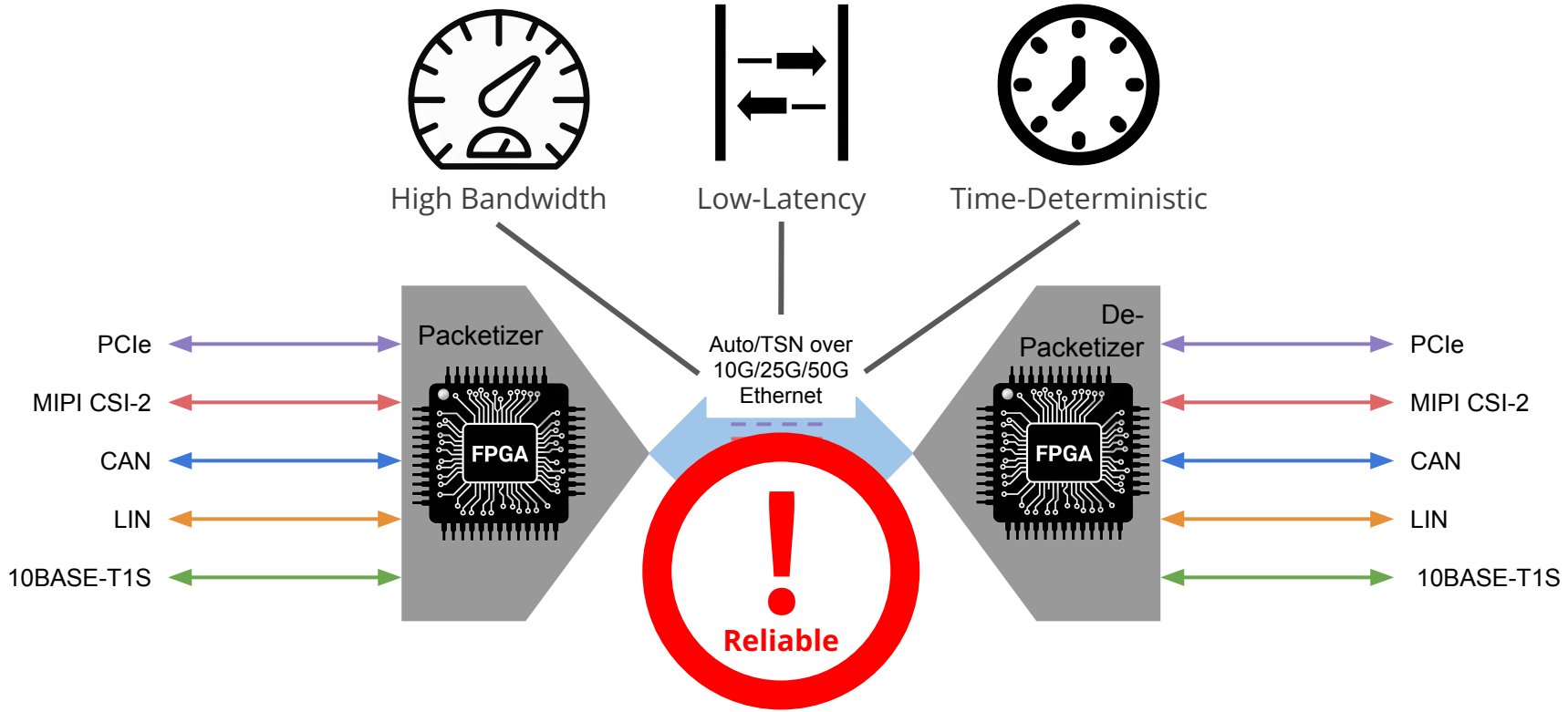

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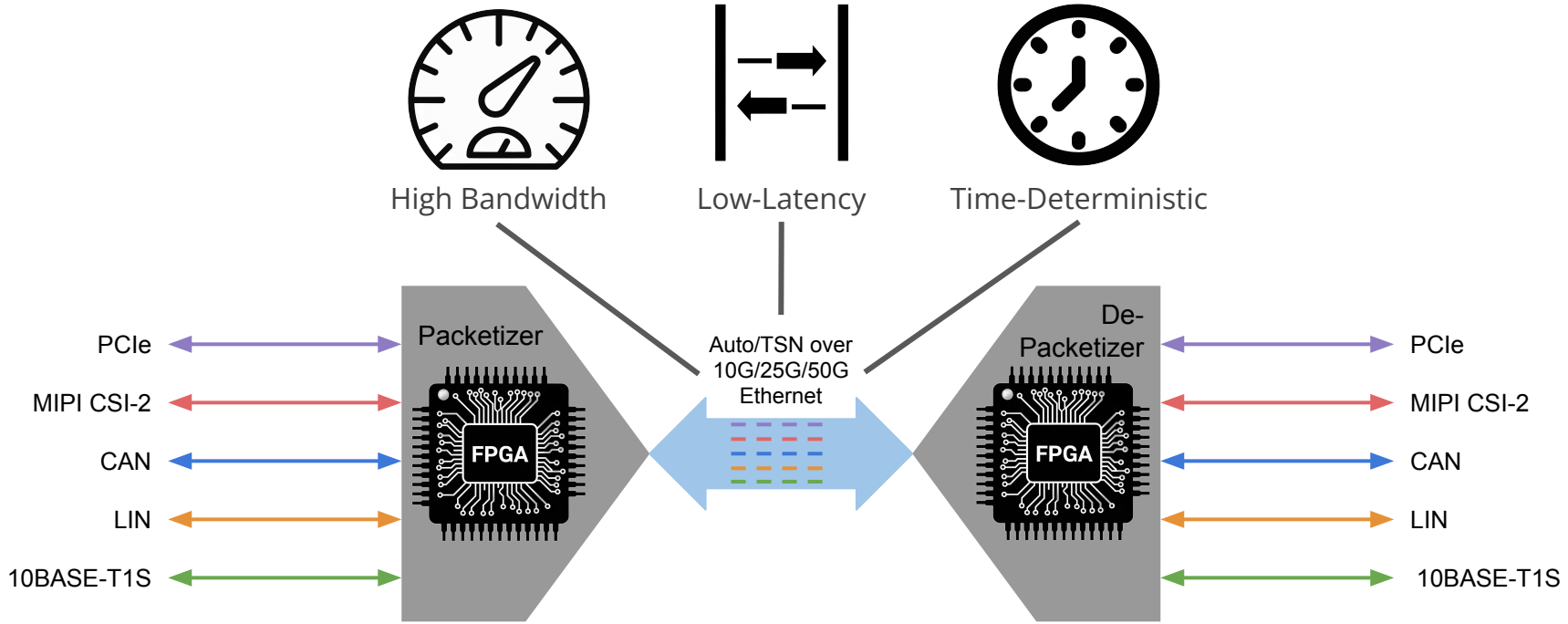
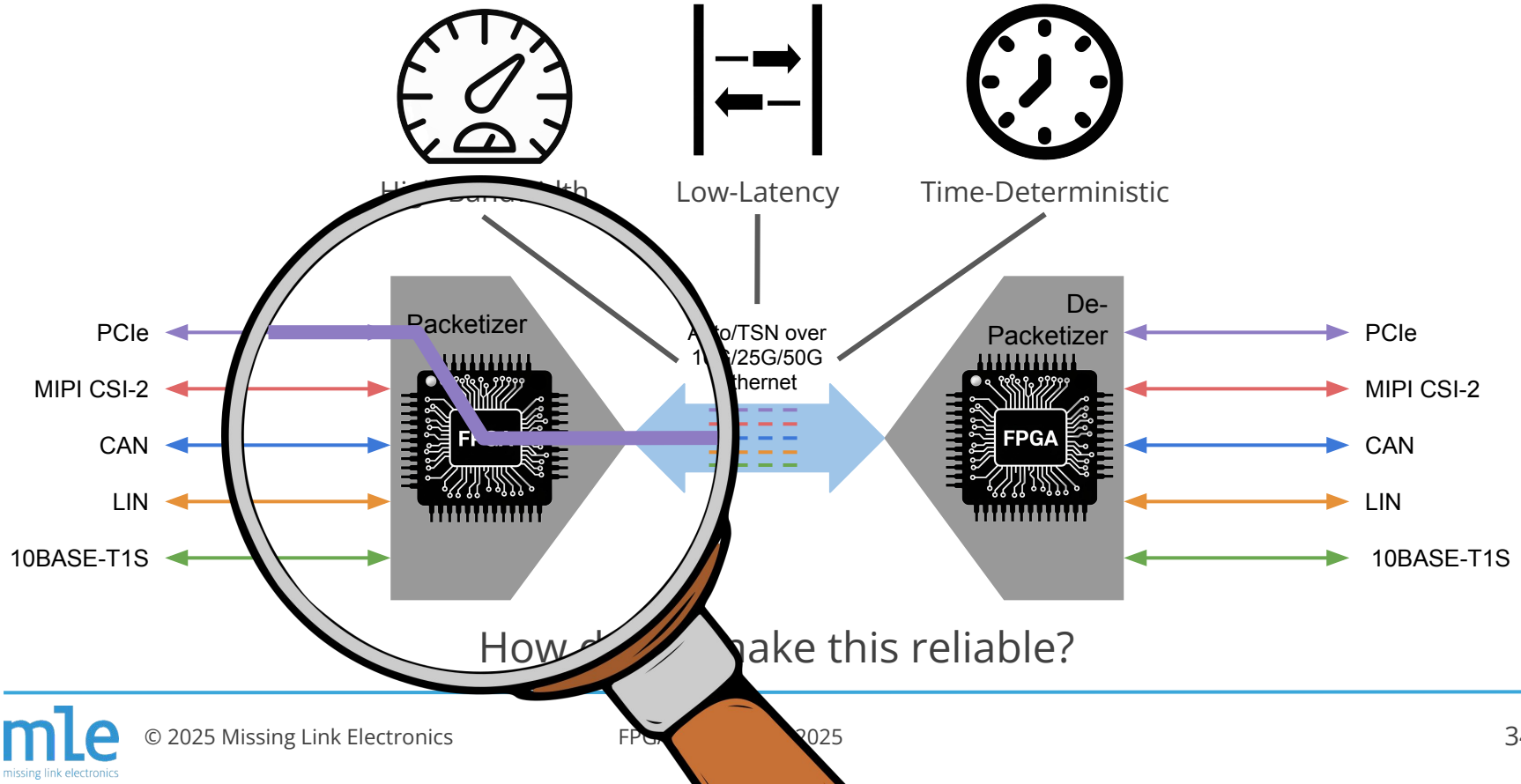


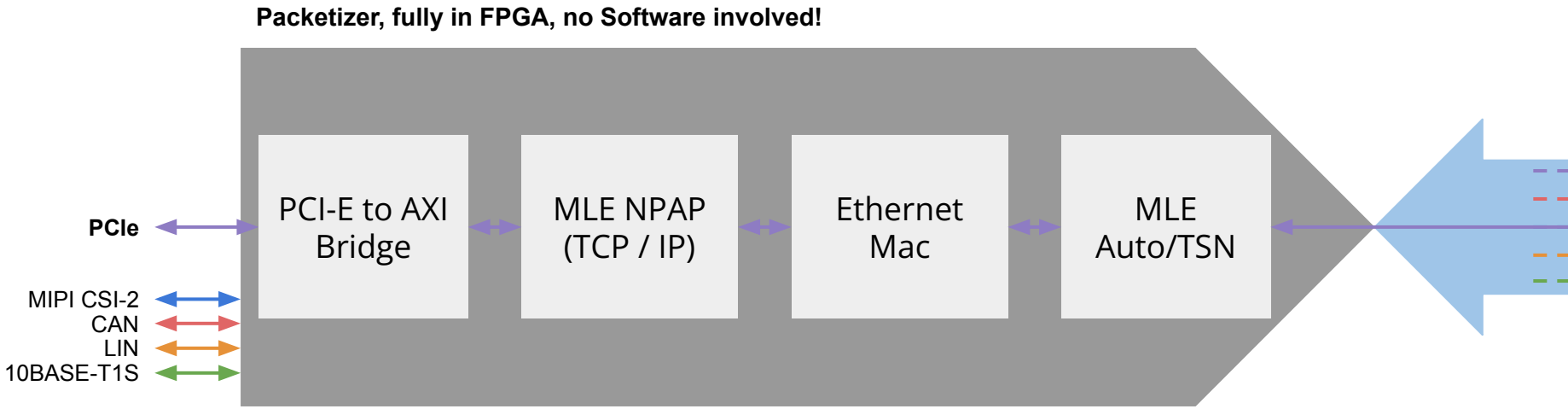
How do we make this reliable?

Auto/TSN for Zone Architectures / in-vehicle network



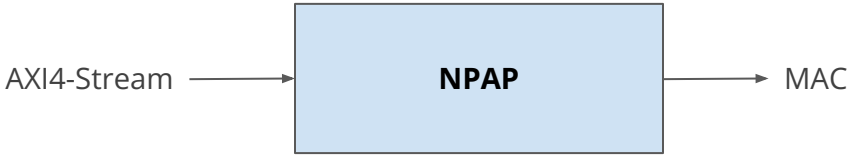
Building a High Bandwidth, Reliable TSN

- Tunnel any Protocol reliably over a Network
- Using proven protocols, fully implemented in Hardware



MLE Network Protocol Accelerator Platform (NPAP)

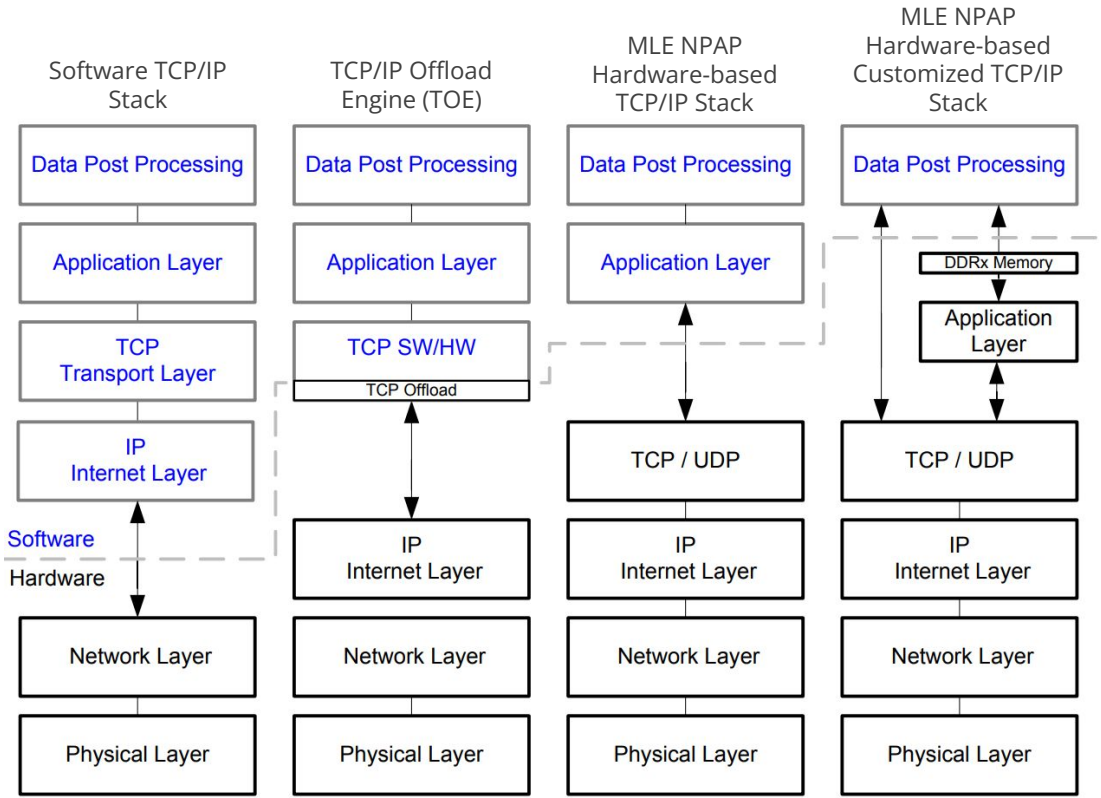
- Network Protocol Accelerator Platform
- TCP / UDP / IP Stack Fully in Hardware



mle missing link electronics + Fraunhofer Heinrich Hertz Institute

Why NPAP? No Software Involved!

Comparison of software and hardware-based TCP/IP stacks



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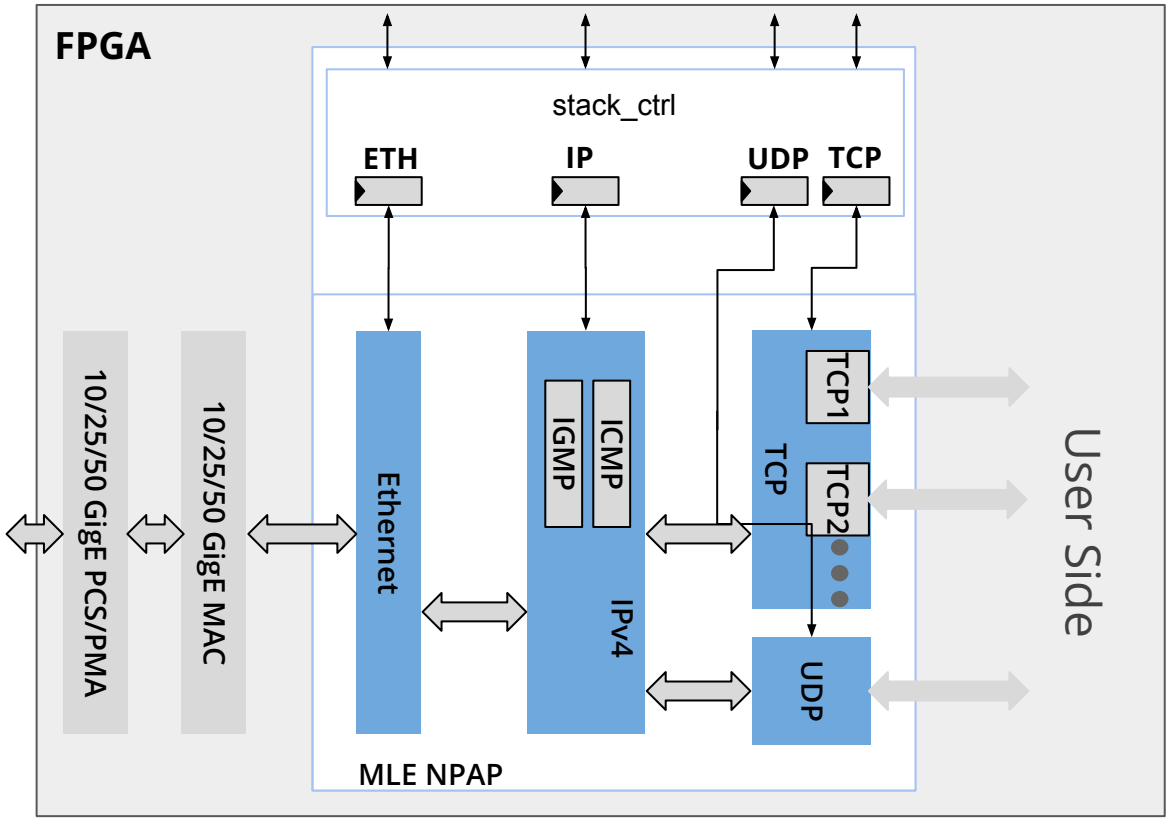
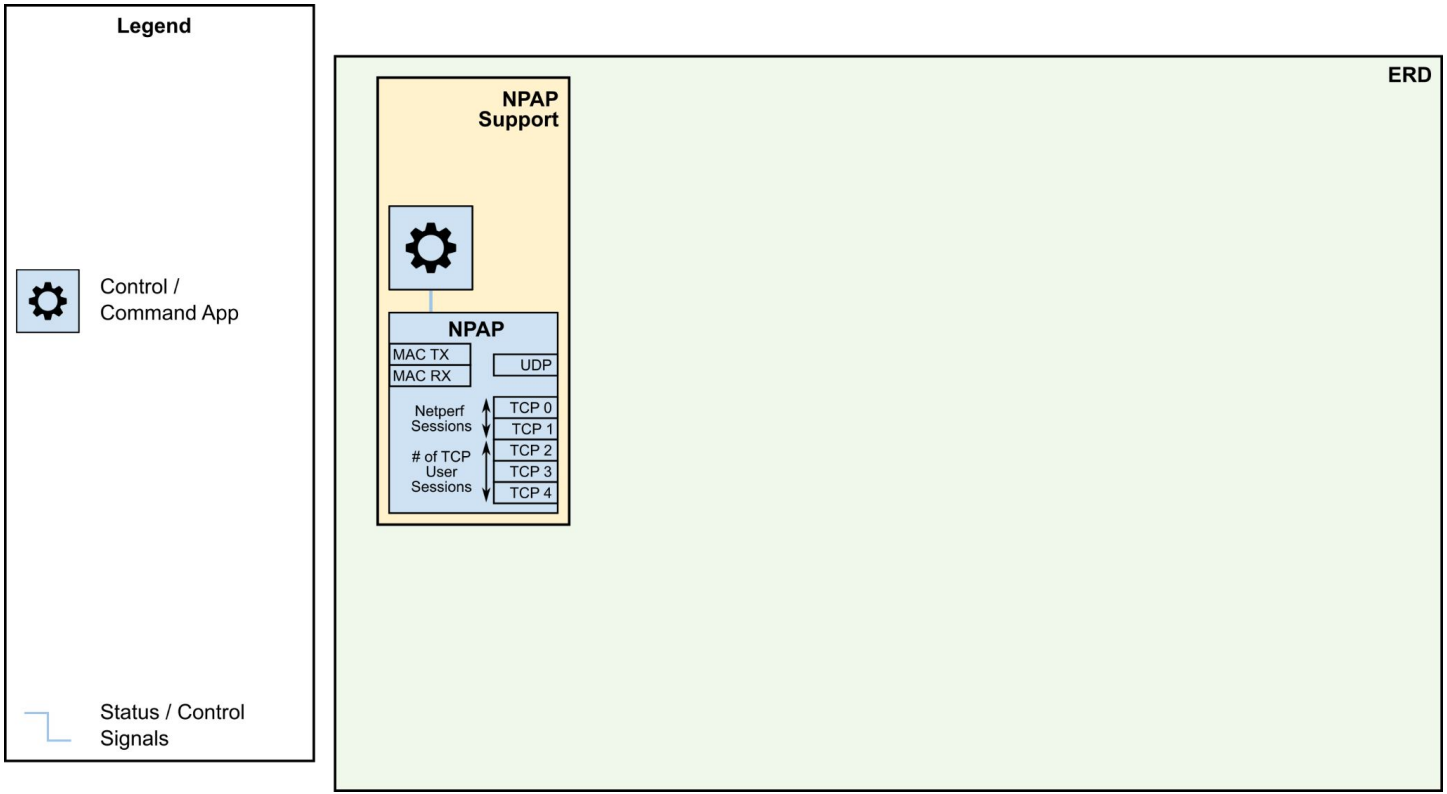


Why NPAP? Well Tested!

Evaluation Reference Design



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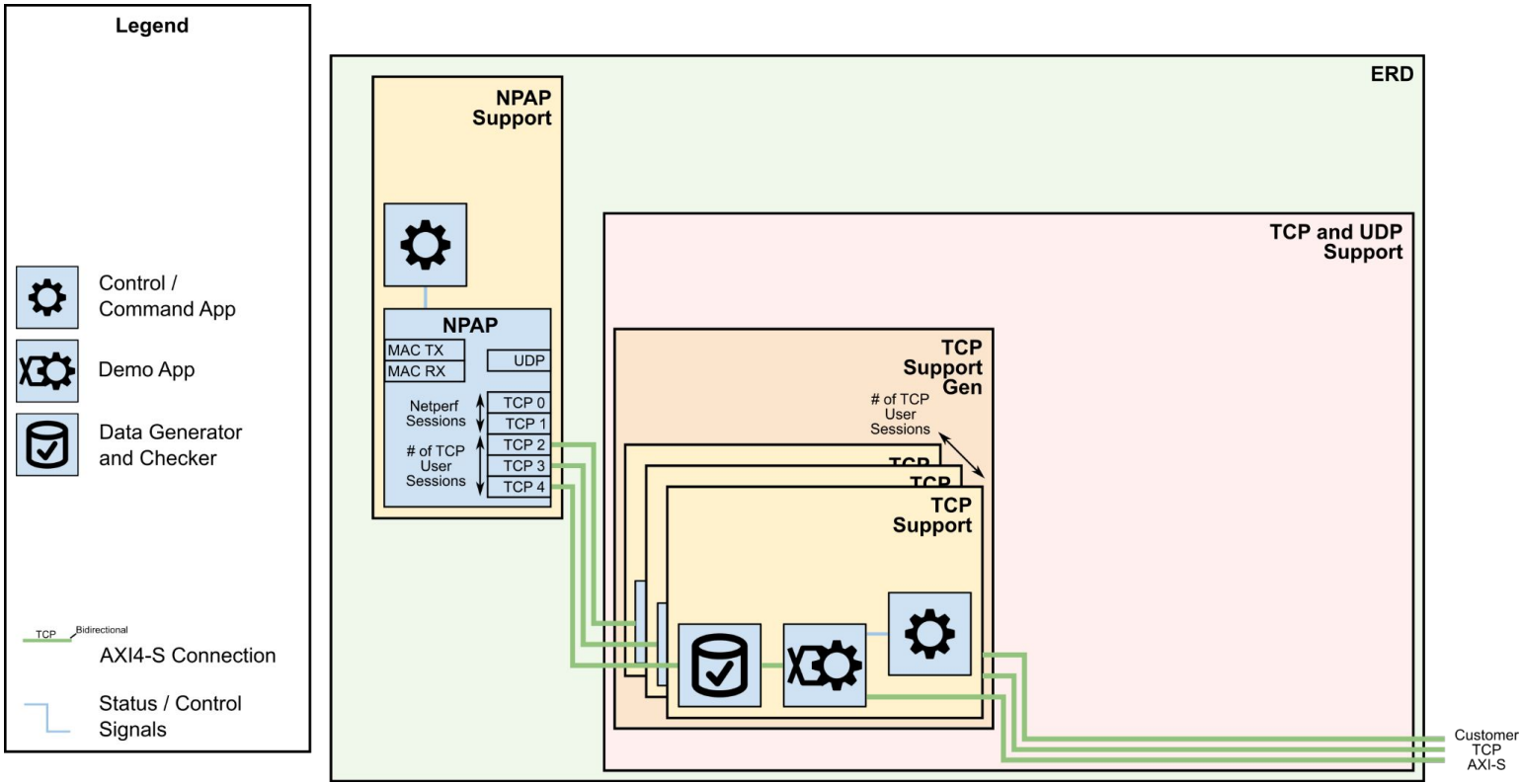

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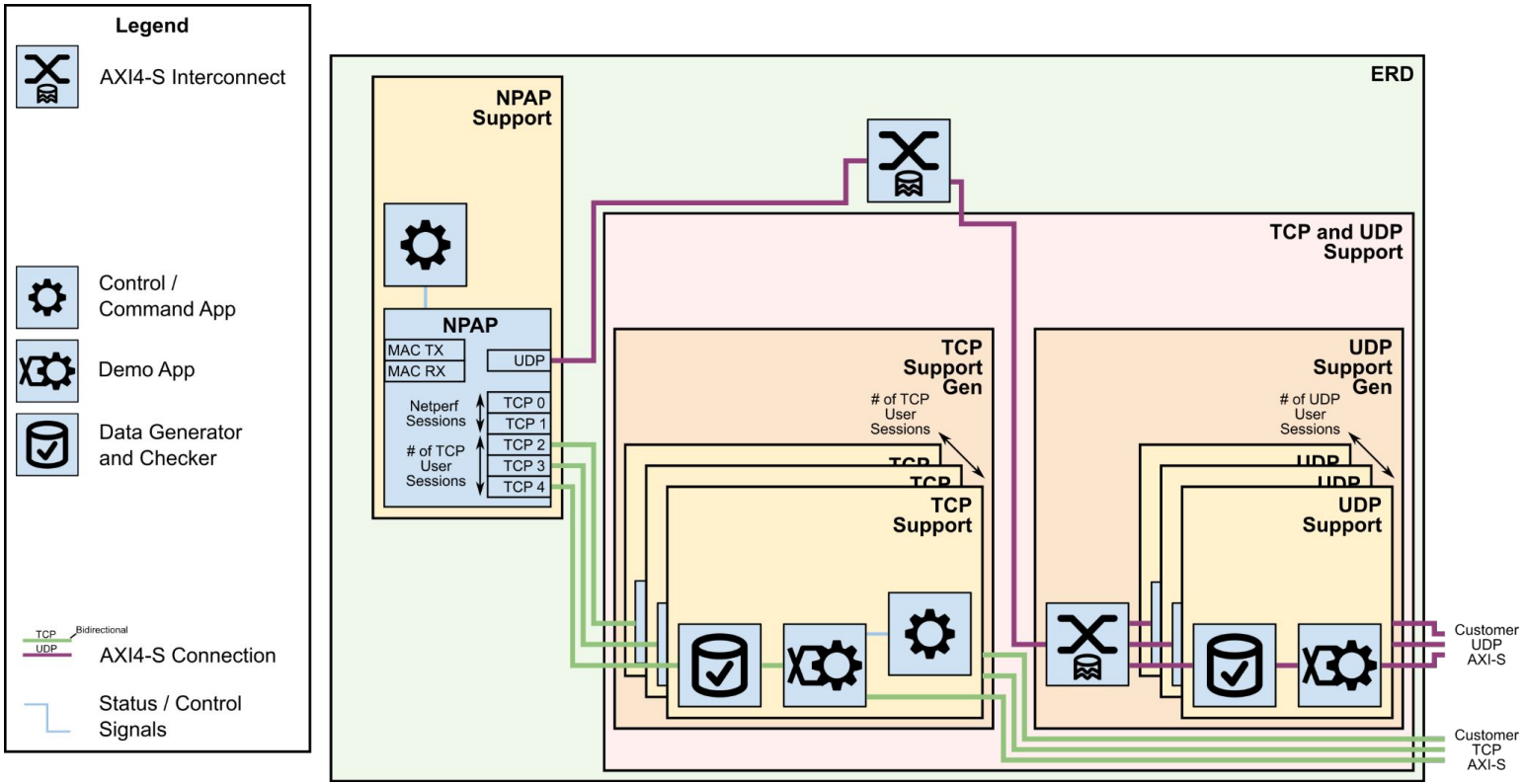

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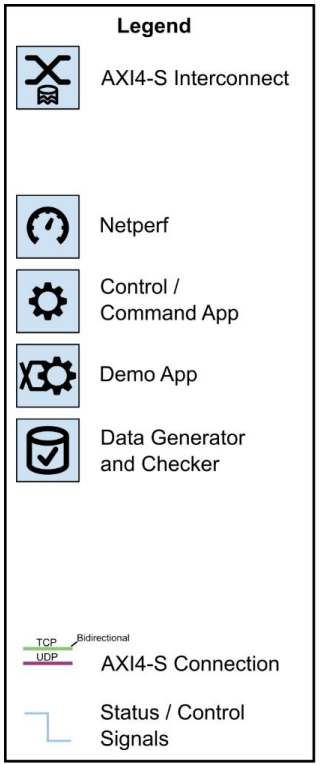

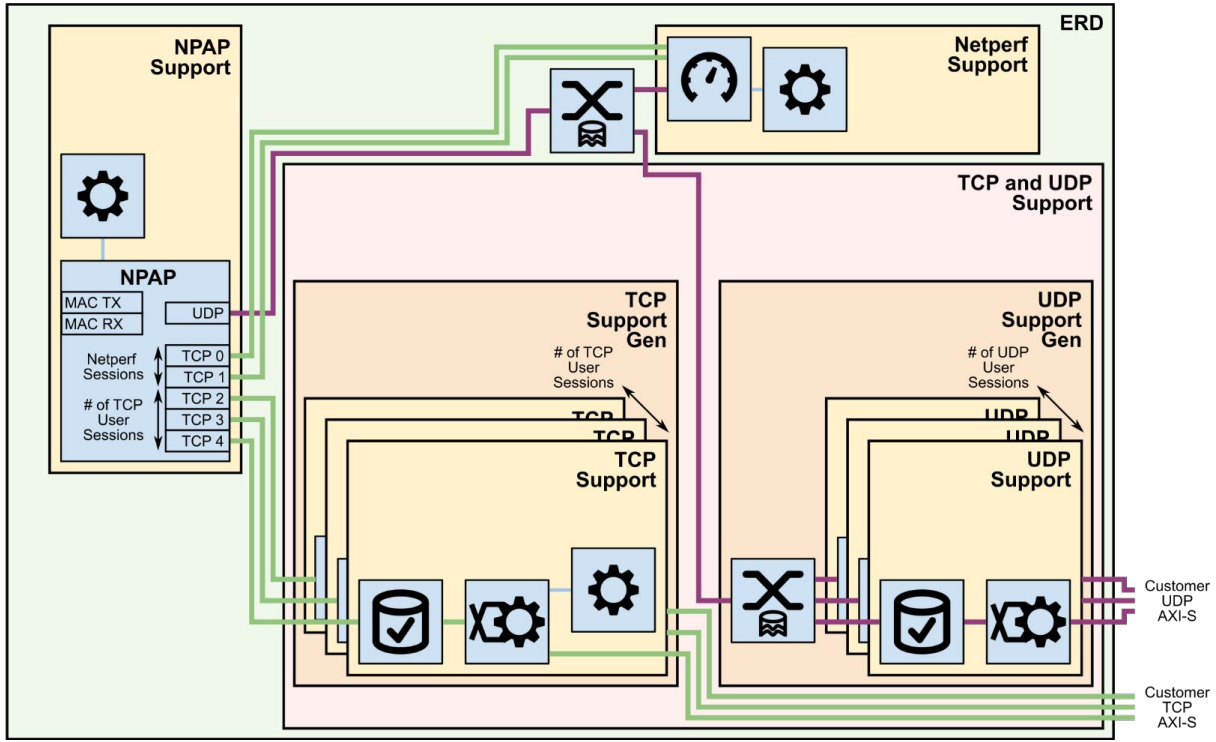

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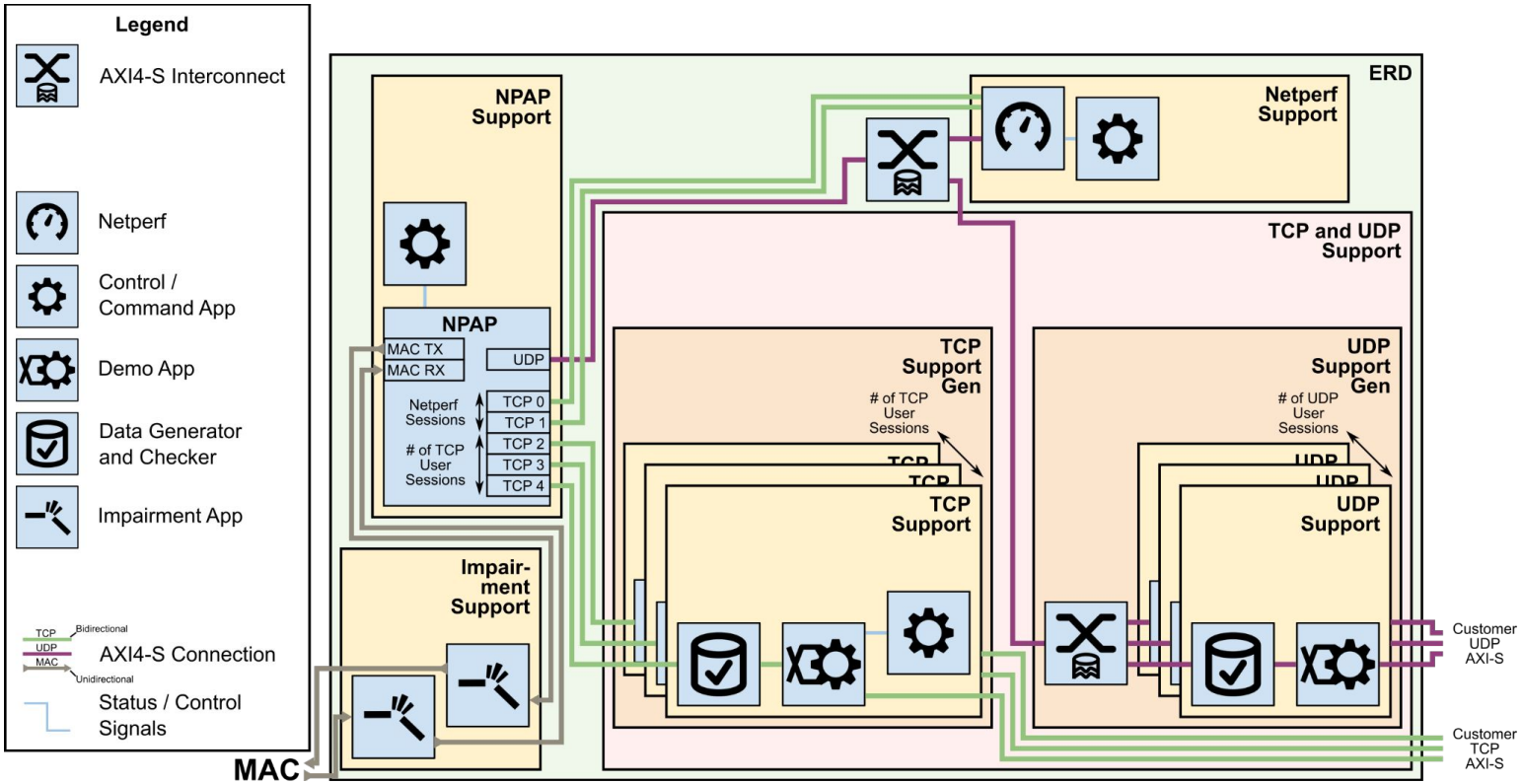

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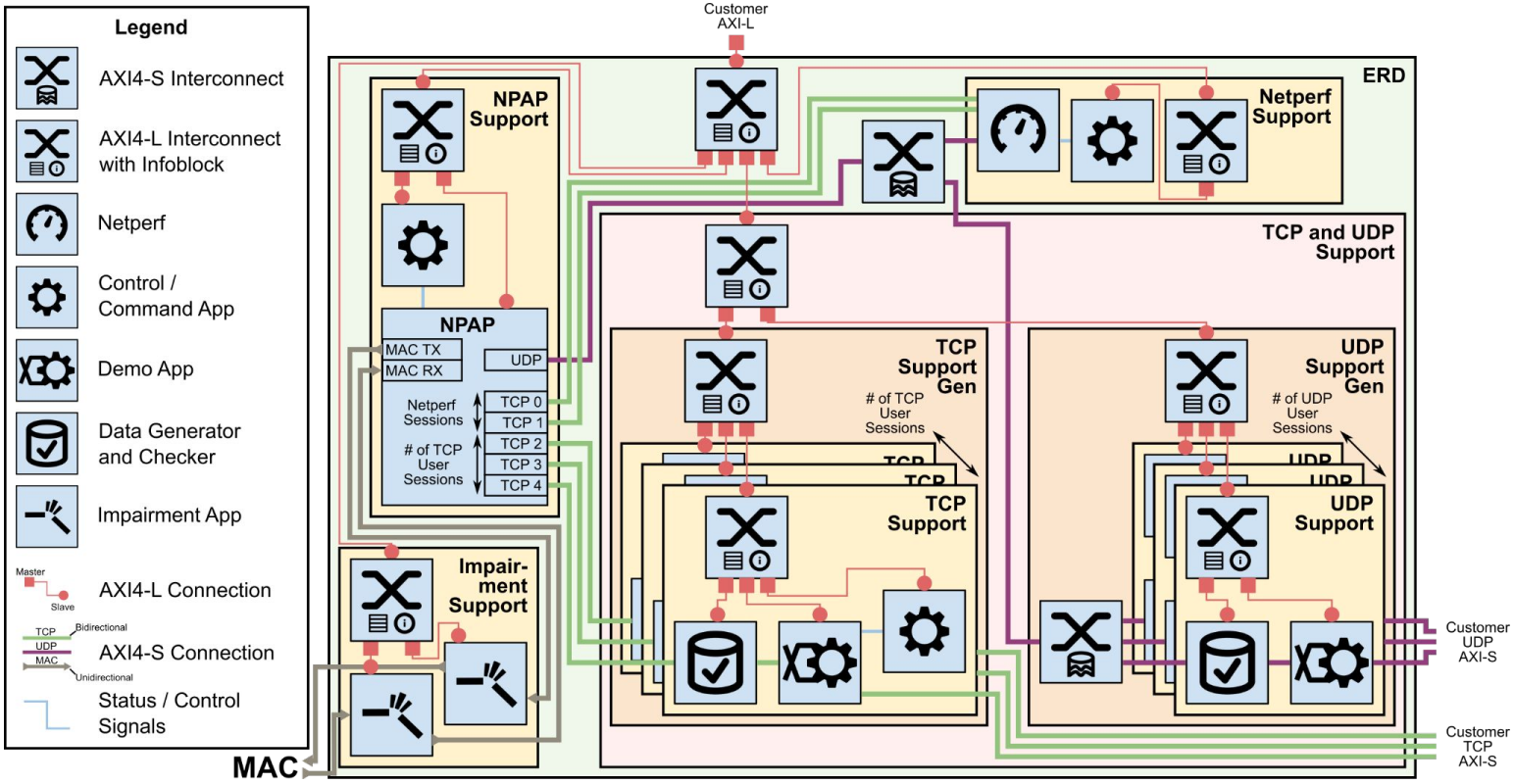
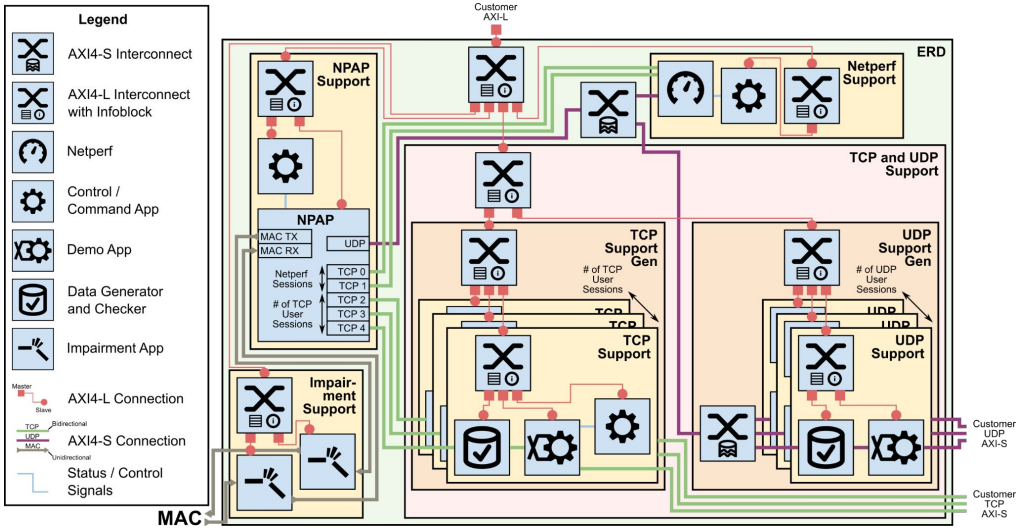


Why NPAP? Well Tested!

Generic Source Code running on

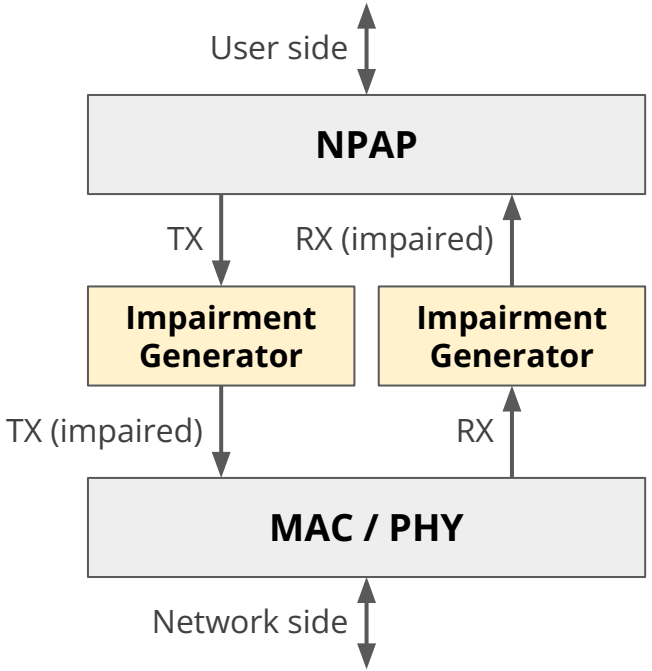
- AMD
  - Virtex 4 to Virtex UltraScale+
  - Kintex to Kintex UltraScale+
  - Artix UltraScale+
  - Zynq-7000
  - Zynq UltraScale+ MPSoC
  - Zynq UltraScale+ RFSoC
  - Versal ACAP Series
- Altera
  - Cyclone IV series
  - Cyclone 10 GX series
  - Stratix V
  - Stratix 10 GX series
  - Agilex 5 D, E Series
  - Agilex 7 F, I, M Series
- Microchip
  - Polarfire and PolarFire SoC
- Lattice
  - Avant-G



Why NPAP? Well Tested!

Impairment Generator

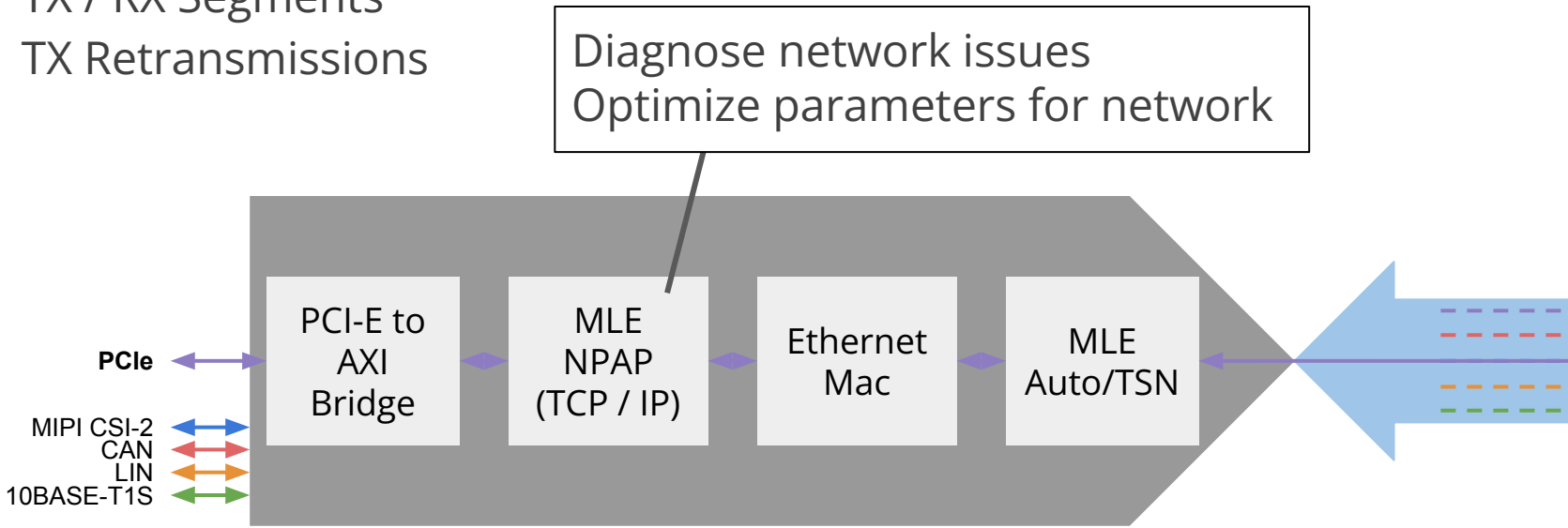
- Designed to emulate packet-level impairments in real-time.
- Injects emulated errors into MAC AXI4-Stream datapaths
- Ideal for verifying the resilience and error-handling capabilities of downstream components



Why NPAP? Well Tested!

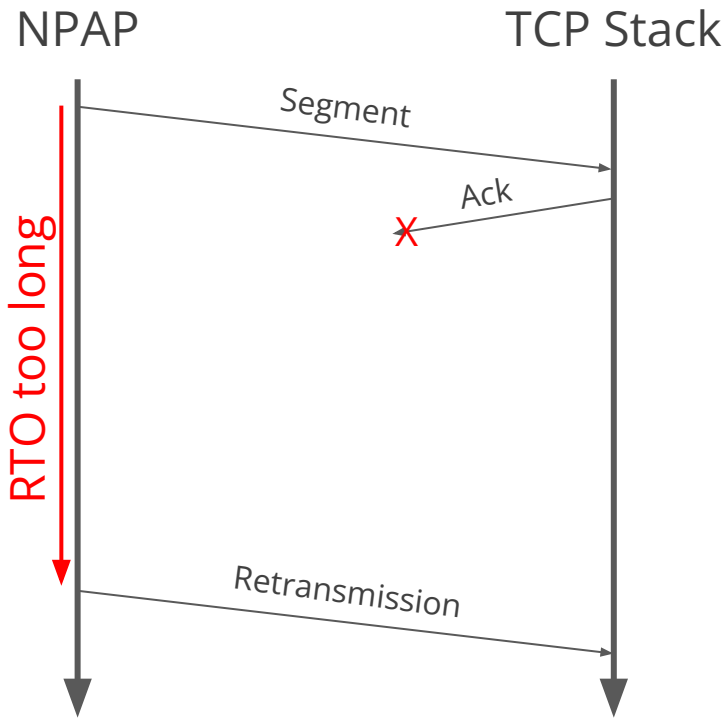
Diagnostics

- Lots of counters accessible via register space, e.g.:
  - TX / RX Segments
  - TX Retransmissions



Why NPAP? Optimization!

- **Reduce unnecessary Latency:**
  - Decrease Retransmission Timeout (RTO)
  - **Check TX Retransmissions**
  - Repeat until TX Retransmissions rise



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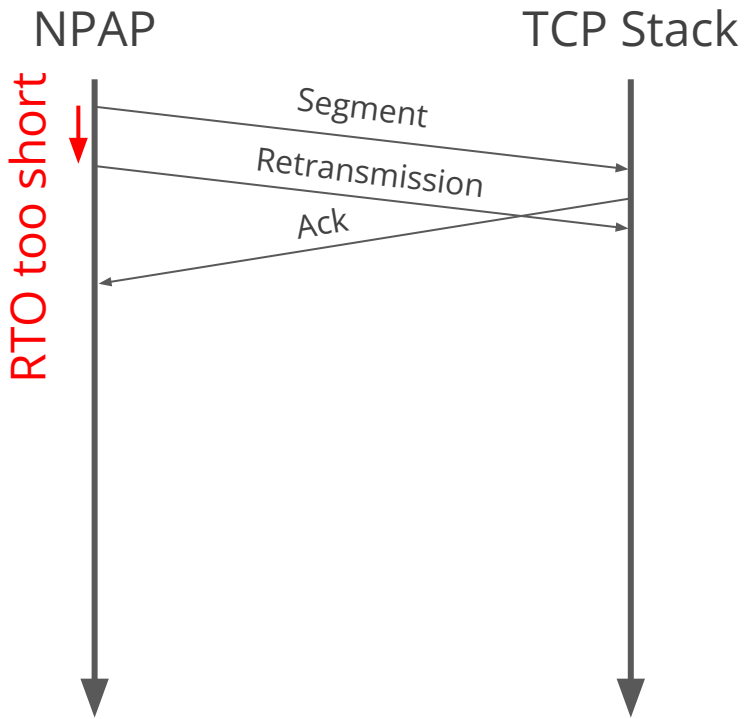

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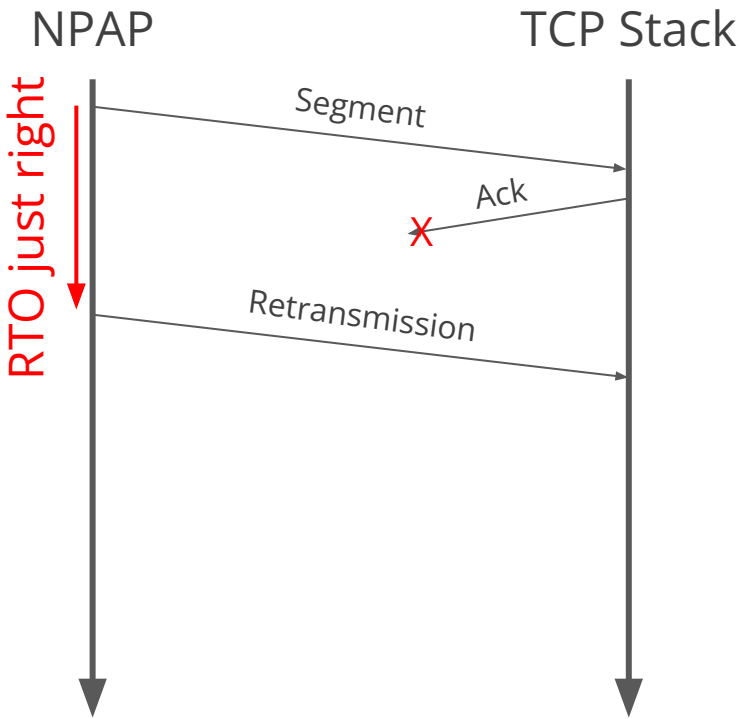
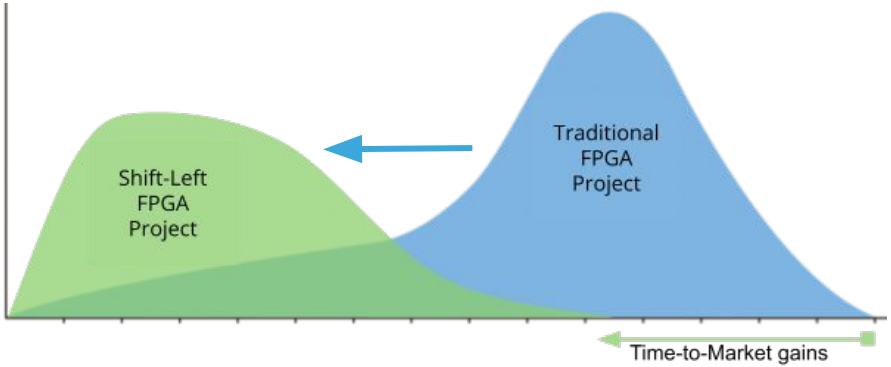
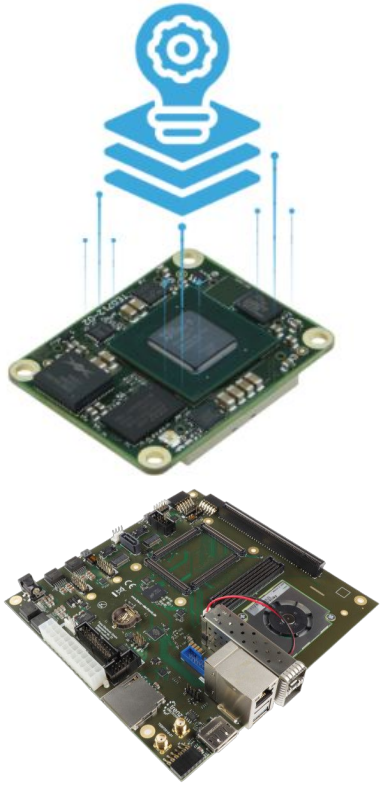


Tackling Technical Challenges: Accelerate FPGA Design

Together with Trenz Electronic we provide Rapid FPGA Prototyping

mle missing link electronics + trenz electronic GmbH





Software development

+

Use off-the-shelf SoM

+

Design Carrier Board

MLE Auto/RPS

Application is for SDV / Zonal Architectures:

- Data-centricity shifts SW development focus from signal to data
- API-first to de-couple and abstract based on vehicle data model
- Modularity & autonomy to enable flexible, scalable SW with high re-use

⇒ Focus on Software Engineers

⇒ Full FPGA System Stack, Ready-to-Run

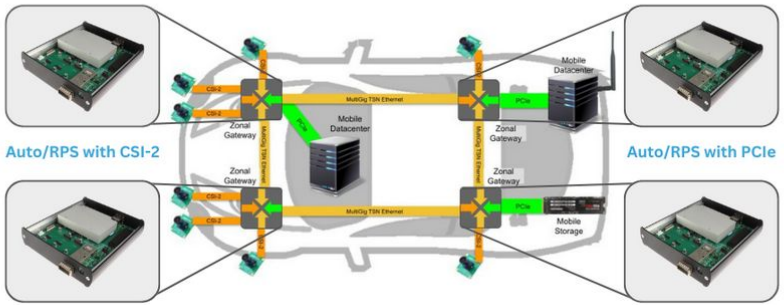
⇒ FPGA is fully transparent (don't have to touch, unless you want to)

Automotive Rapid Prototyping System (Auto/RPS)

MLE provides an FPGA-based Rapid Prototyping System (RPS) catering to the specific needs of automotive engineers designing next-generation Zone Based Architectures.

MLE Auto/RPS enables automotive system engineers to design and to validate software-defined vehicle (SDV) functions along with MLE Auto/TSN in-vehicle networking.

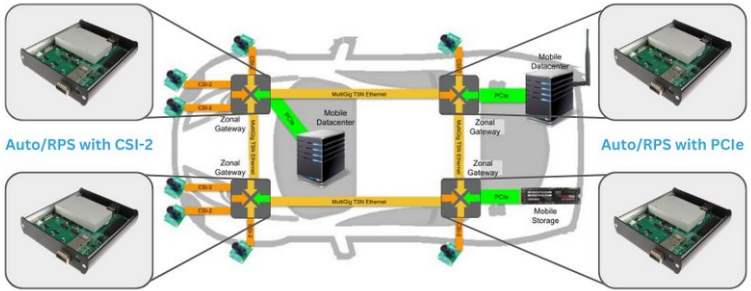
MLE Auto/RPS was designed as a shortcut into A-sample hardware development of Zonal Gateways / ECUs and implements an FPGA Full System Stack based on the Trenz Electronic TE0950-02 SoC-FPGA Development Kit featuring the AMD Versal AI Edge FPGA, and an automotive FPGA subsystem from MLE.



MLE Auto/RPS

Auto/RPS supports connectivity for (almost) all relevant I/O interfaces:

- 1 Gig Ethernet (for example for remote access and housekeeping)
- USB 2.0 for JTAG and console (supports even keyboard and mouse)
- 2x ports for 25G Ethernet (up to 4 ports optional)
- MIPI CSI-2 x2 Camera Input (optional)
- Up to 2x CAN-FD (via CRUVI HS) (optional)
- Up to 2x CAN 2.0B (via CRUVI HS) (optional)
- NVMe M.2 SSD (optional via Opsero FMC M.2 adapter)
- PCIe 4.0 x4 via 4x GTYP (optional, for high-speed debugging etc)



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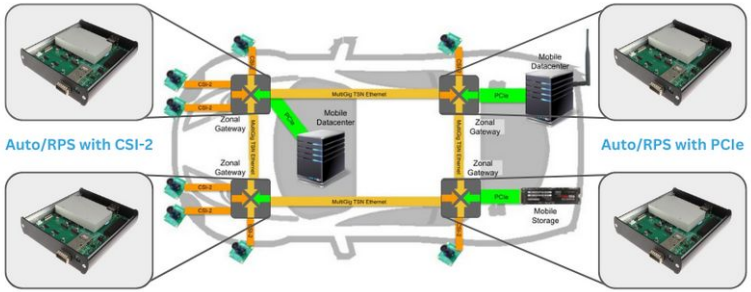
Working on a V2 together with Trenz to support even more I/O interfaces



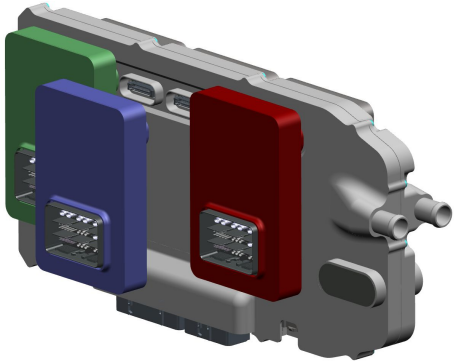
Auto/TSN for Zone Architectures / in-vehicle network

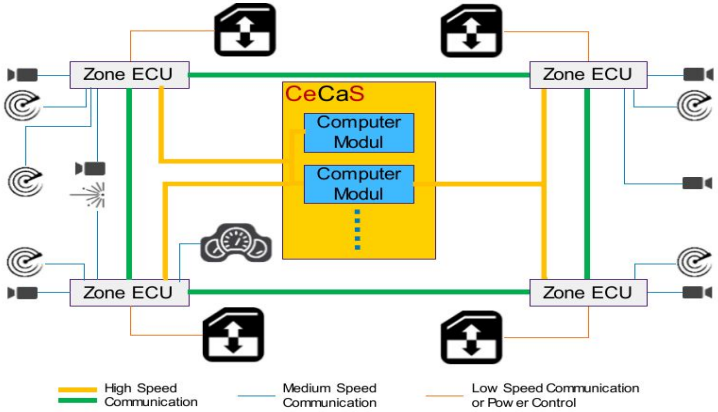
BMBF CeCaS

Budget: 88 Mio EUR

Key Objectives:

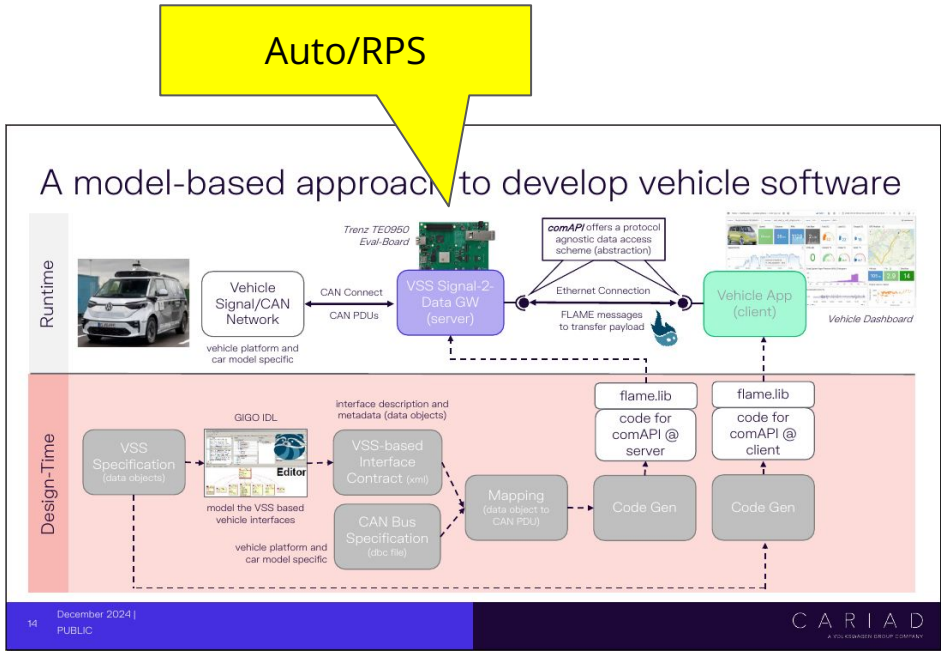
- Zone-base architecture
- Auto SoC / Chiplets
- Mechanical / thermal





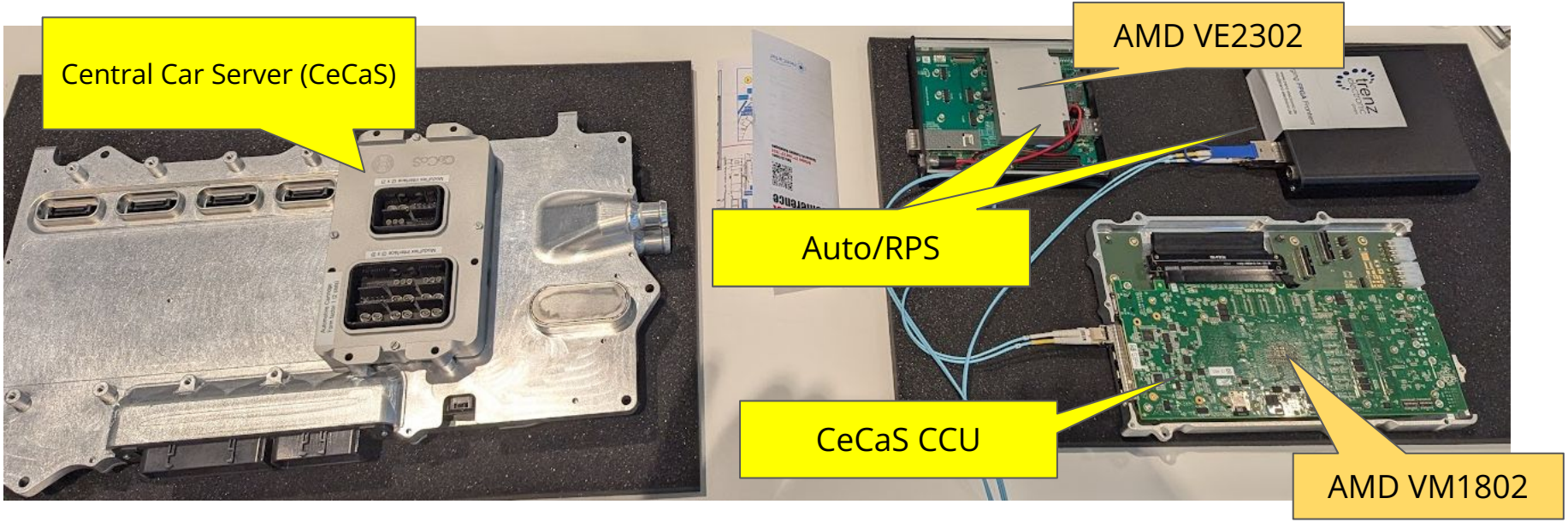
- AMD Versal VM1802 for “emulating” ADAS compute and connectivity
- AMD Versal VE2303 for “emulating” Zone ECUs / gateways

MLE Auto/RPS in Action as Zone Controller



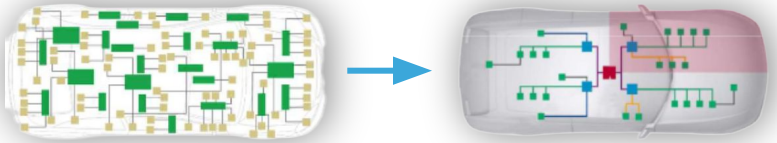
Auto/RPS in Action

Presented at BOSCH Automotive Ethernet Conference, Oct 2024, Renningen



Conclusion

Turning today's automotive wiring mess into tomorrow's automotive architecture is doable by using a Zone Based Architecture.



However:

1. Zonal architectures require fast networks and rapid development.
2. We provide the technology: Reliable Networking using ultra-fast TSN.
3. We provide the methodology: Auto/RPS for rapid FPGA prototyping.

Thank you

Any questions?

Contact:

Maximilian Sokol

max.sokol@missinglinkelectronics.com

Andreas Schuler

Andreas.schuler@missinglinkelectronics.com

Missing Link Electronics

Industriestraße 10
89231 Neu-Ulm

www.missinglinkelectronics.com