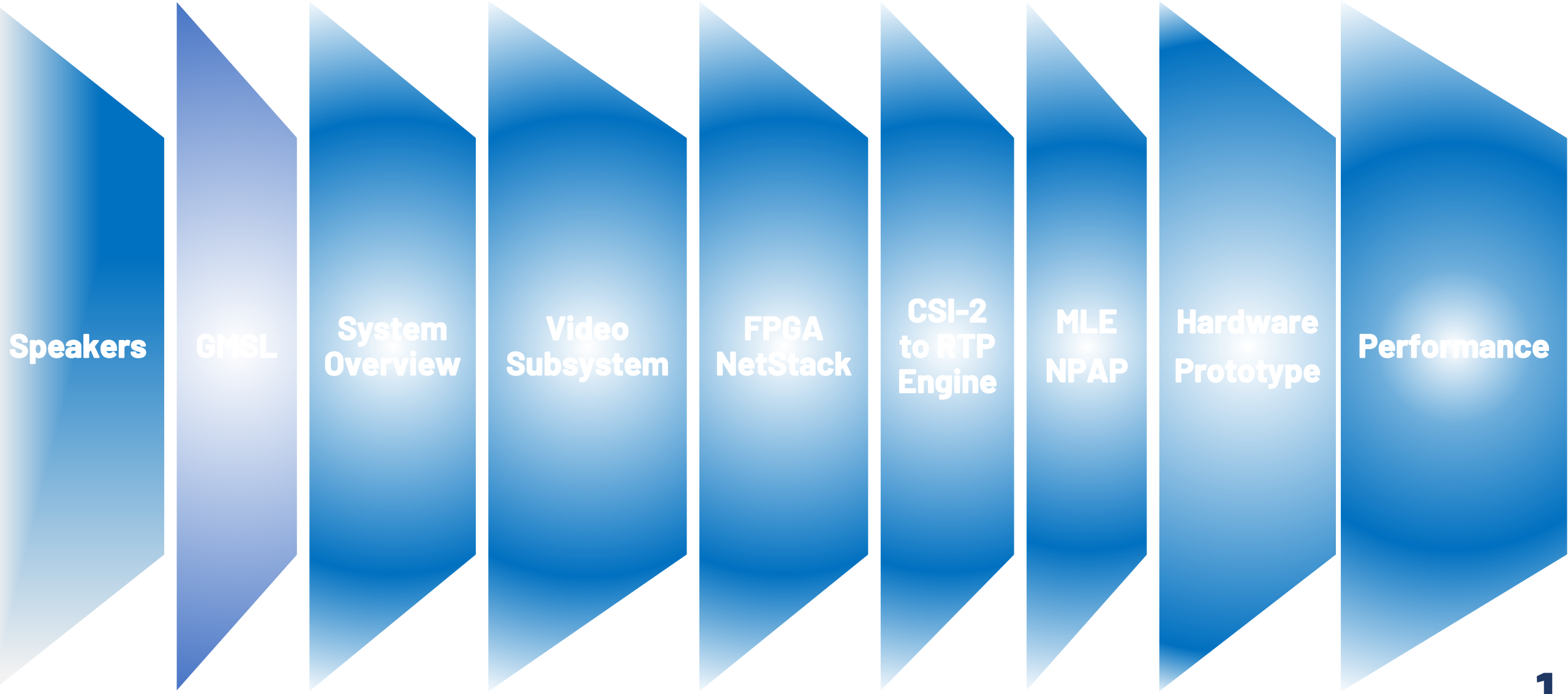
FPGA-based Highly Configurable and Low-Latency Multi GMSL Camera 10GbE RTP Streaming Performance and Design Choices

Agenda



Speakers

Alin-Tudor Sferle

Analog Devices Romania

Friedrich Maximilian Sokol (Ulrich Langenbach)

Missing Link Electronics Germany

What is GMSL

Gigabit Multimedia Serial Link

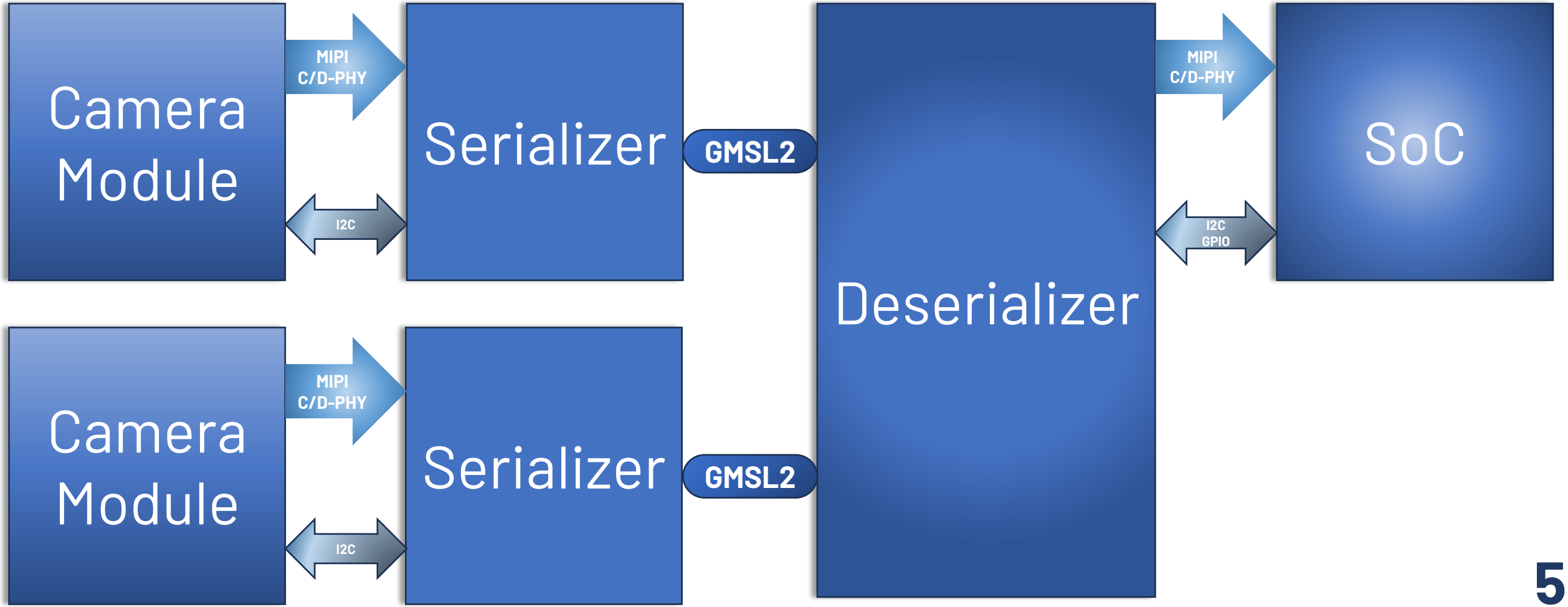
- High-Speed Video Link over a Single Wire
- Scalable SerDes Technology
- Camera/Display Use-Cases
- Multimarket Applications
- Up to 6/12 Gbps in GMSL2/3
- Since 2004

GMSL2
For Cameras

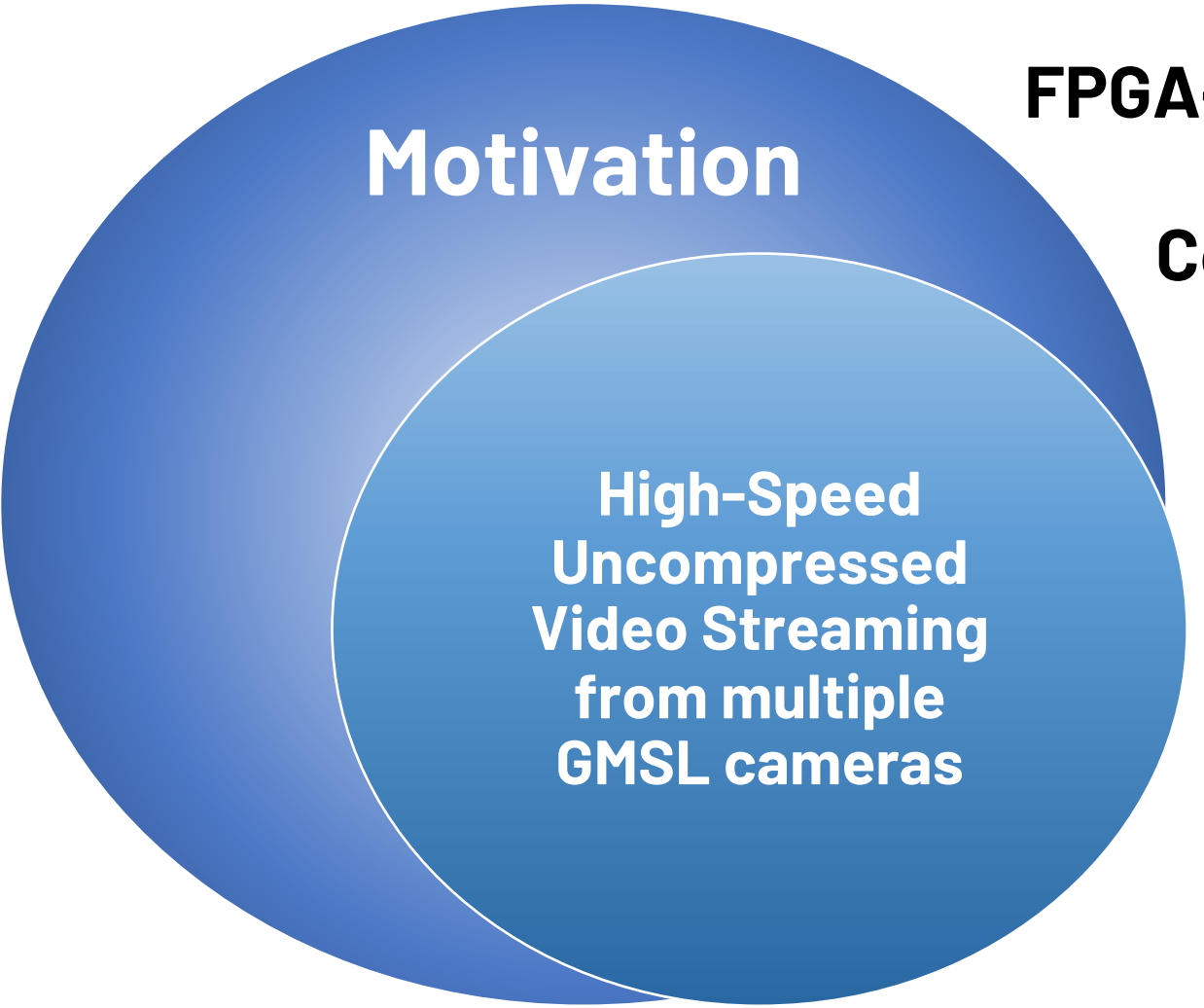
Serializer	Deserializer
One/Two Input Ports	One/Two/Four Input Ports
Parallel/CSI Input Interface	Parallel/CSI Output Interface
GMSL over Coax/STP*	GMSL over Coax/STP*
Virtual Channel Option	Virtual Channel Option
Power/GPIOs/I2C/Video over GMSL	Power/GPIOs/I2C/Video over GMSL

*STP - Shielded Twisted-Pair

GMSL2
Camera Pipeline Example



System Overview



Use of Low Latency FPGA-based UDP/IPv4 Network Accelerator

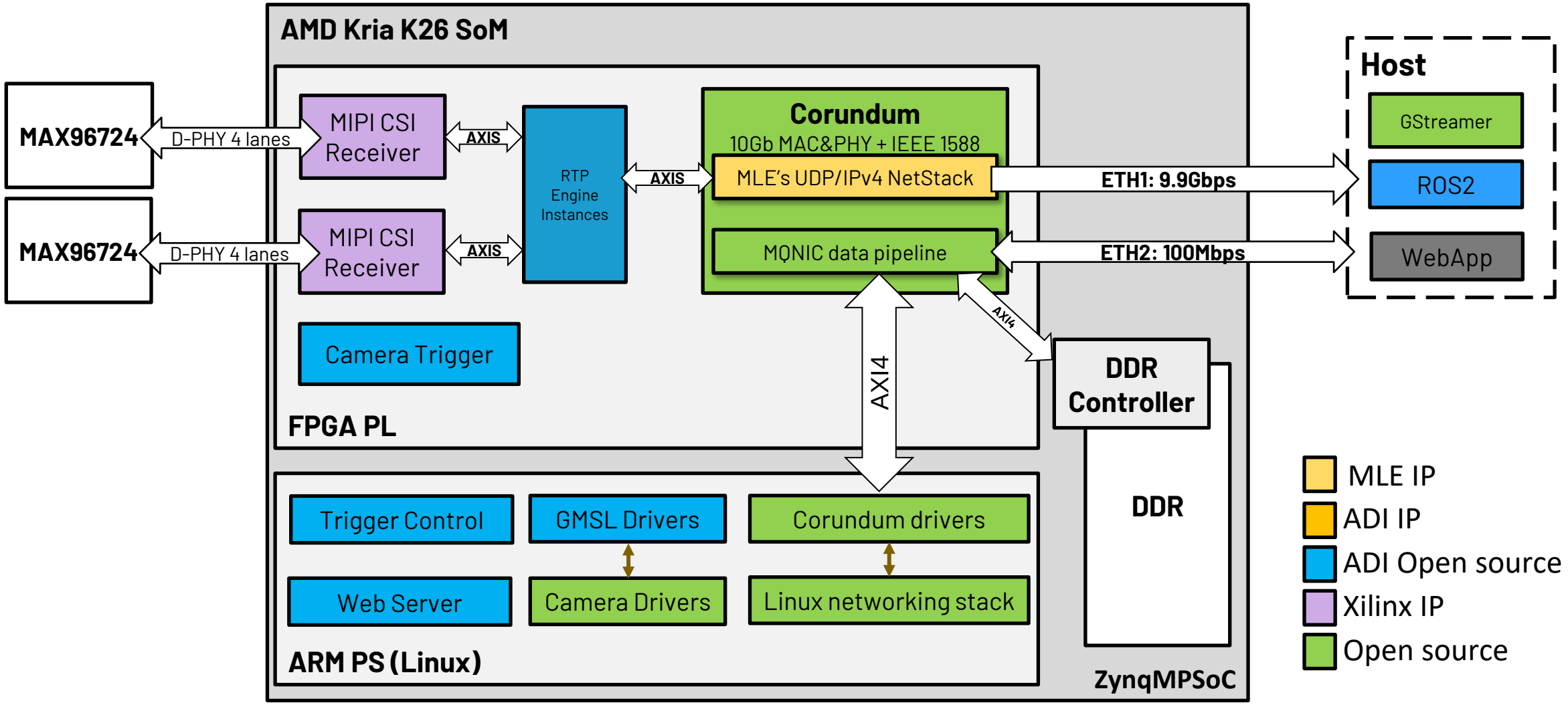
Configurable GMSL Camera Triggering

IEEE-1588-based Timestamping

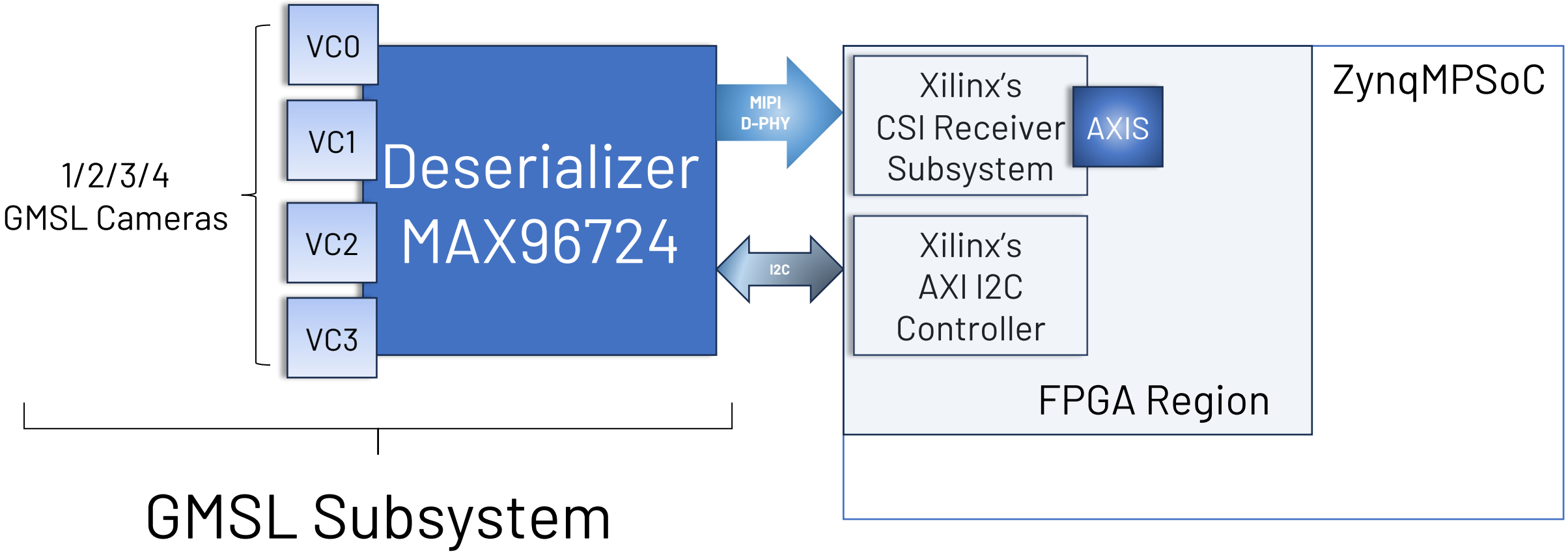
Interrupt-free Network Accelerators Design

NIC + FPGA-accelerated Video Streaming on same 10G PHY Link

Prototype Overview



Video Subsystem – P1



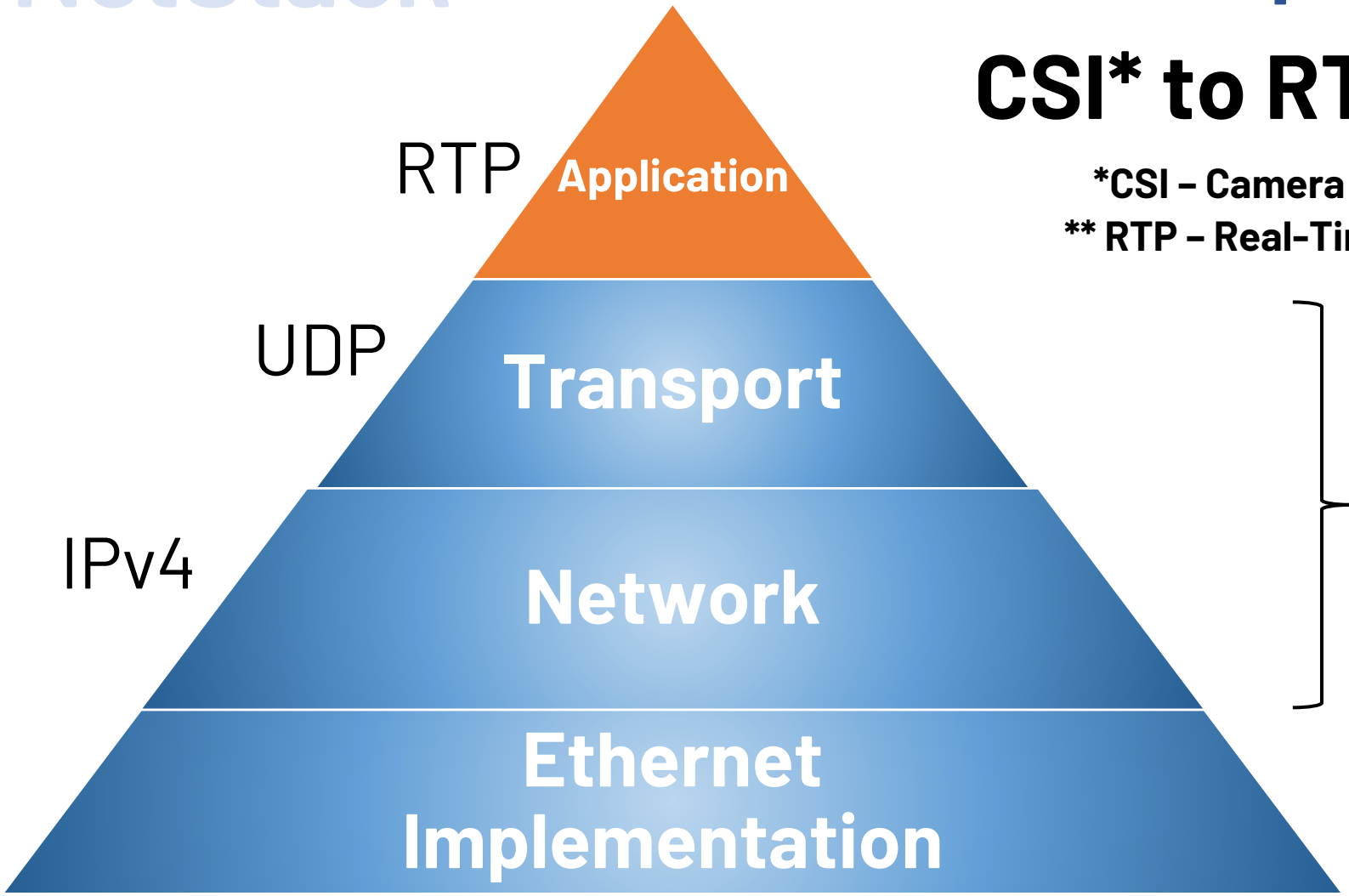
Video Subsystem – P2

- **HDL/FPGA Support**
  - Xilinx's MIPI CSI Receiver Subsystem:
    - 4 Lanes D-PHY [1500 Mbps] + YUV422 Input Support
    - Up to 4 VCs decoding
    - V4L2-compliant
  - Xilinx's AXI I2C Controller:
    - For the GMSL Subsystem's Components
- **Linux Support**
  - V4L2-subdevices: Sensor, Serializer, Deserializer, CSI Receiver

RFC-Compliant Implementation

CSI* to RTP** Engine

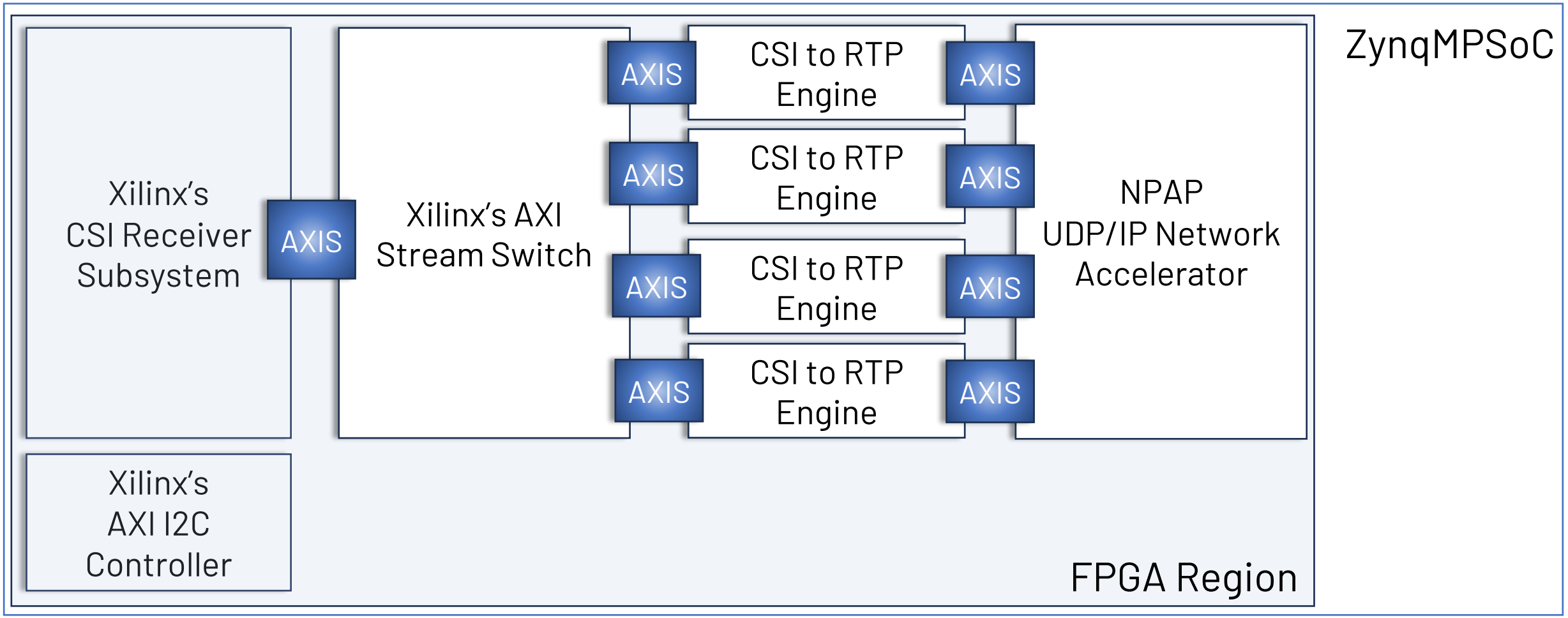
*CSI – Camera Serial Interface
** RTP – Real-Time Transport Protocol



MLE's NPAP

Corundum

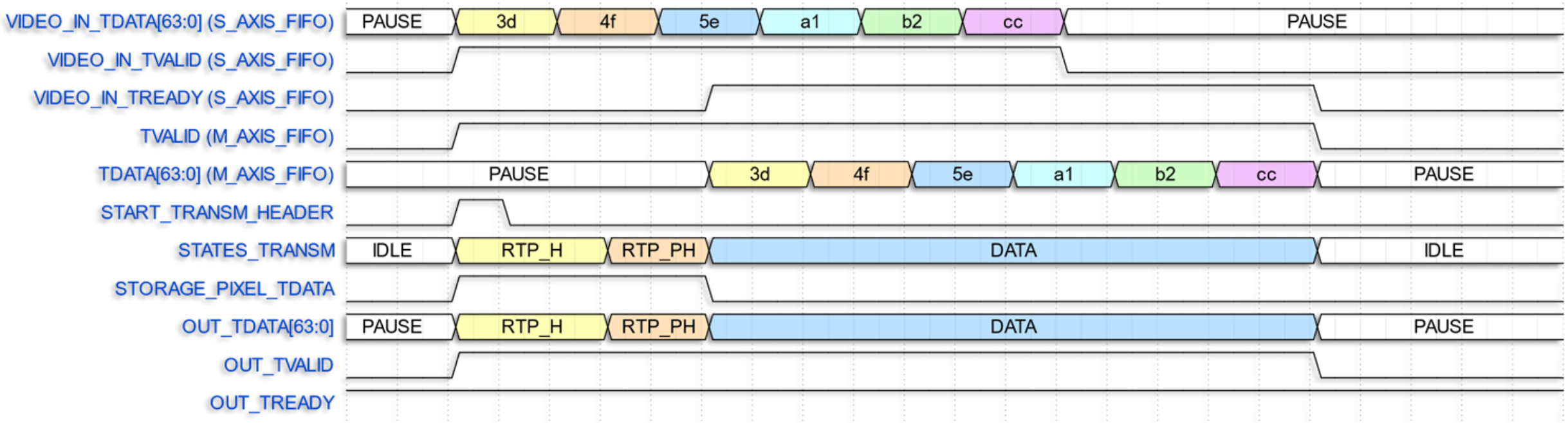
CSI to RTP Engine – P1



CSI to RTP Engine – P2

- SW controllable through AXI4-Lite
- YUV422 format support
- RFC-compliant design - **RFC4175** + **RFC3550**
- Configurable number of lines and pixels per line at runtime
- 1 Line per RTP packet leveraging on Jumbo Frames

CSI to RTP
Conversion – P1

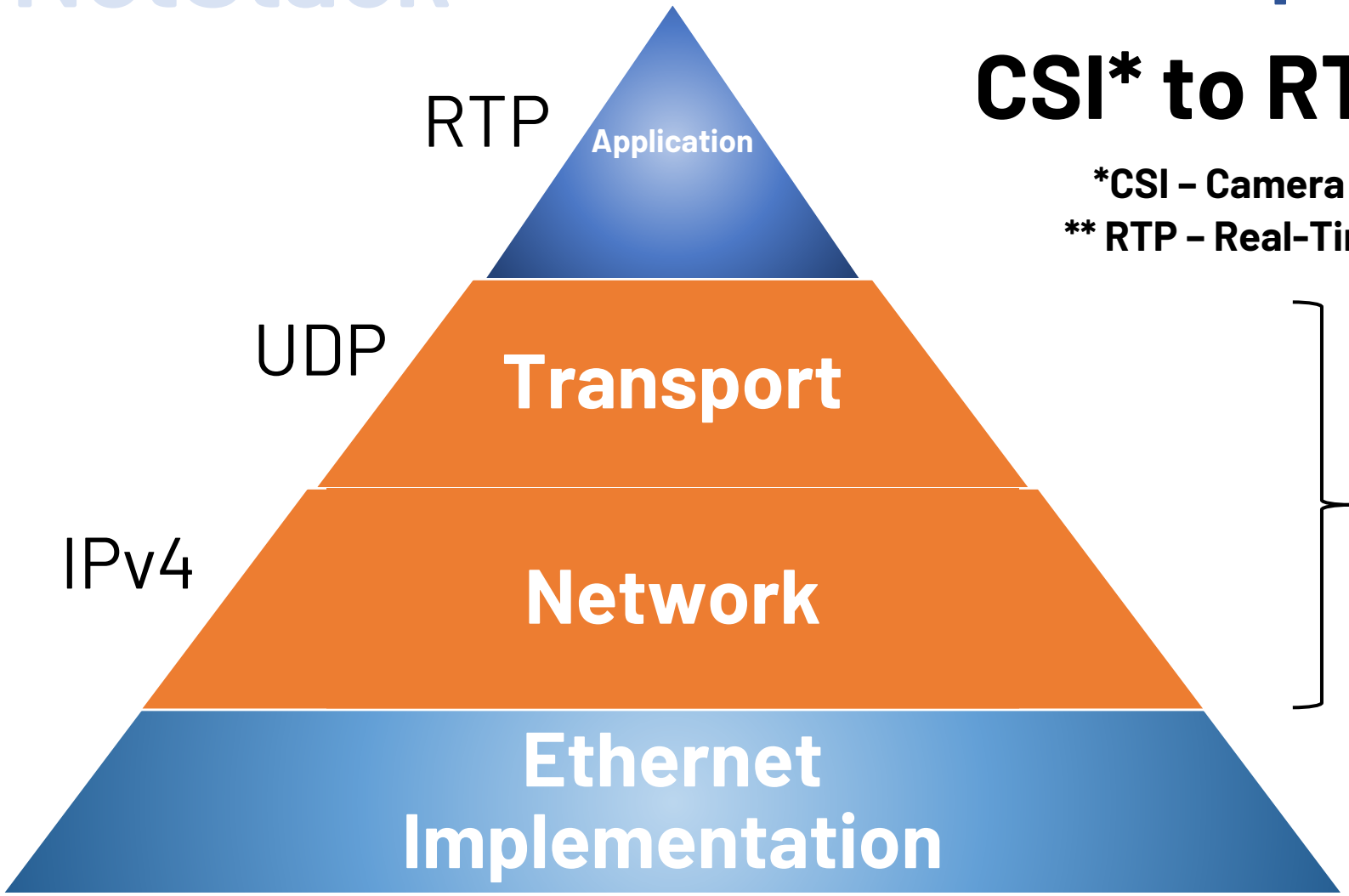


* RTP_H – RTP Header
* RTP_PH – RTP Payload Header
* PAUSE - Blanking Time [CSI-2]

CSI to RTP Conversion – P2

- Conversion of 1 video line to 1 RTP packet
- Internal Buffers designed for Header Transmission & Congestion on the 10 GbE link
- AXI Streaming compliant video to RTP conversion
- Designed as a packaged IP (Vivado's Block Design)

RFC-Compliant Implementation



CSI* to RTP** Engine

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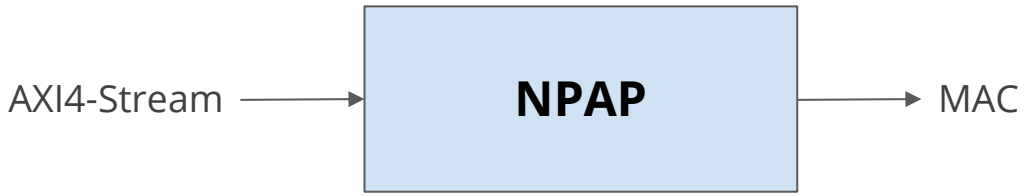
** RTP – Real-Time Transport Protocol

MLE's NPAP

Corundum

NPAP

- MLE Network Protocol Accelerator Platform (NPAP)
- TCP / UDP / IP Stack Fully in Hardware
- 1 / 2.5 / 5 / 10 / 25 / 40 / 50 / 100 Gigabit Ethernet Interface
- Full-duplex with 128 bit wide bidirectional datapath
- Designed fully in HDL
- Platform independent



missing link electronics

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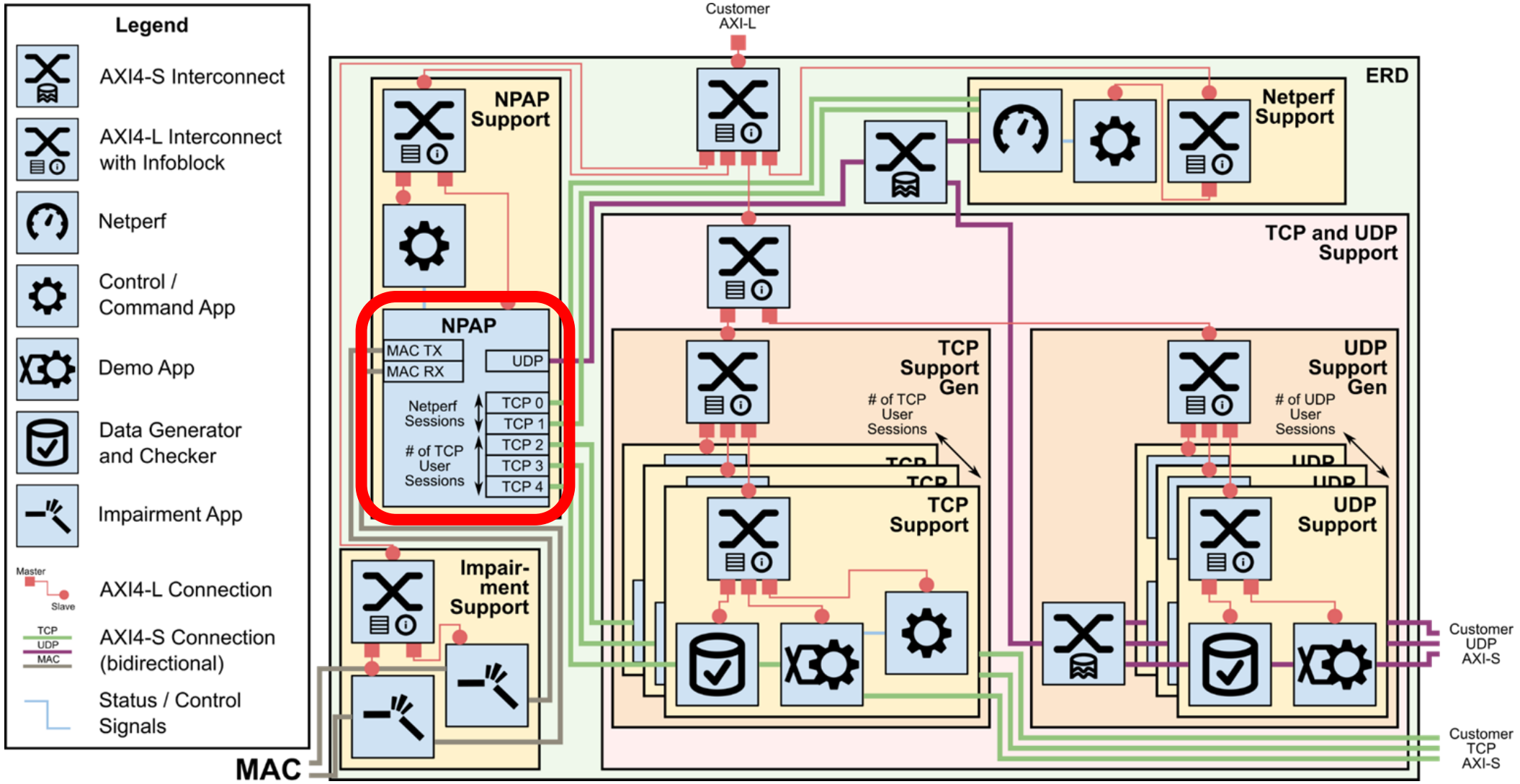
Fraunhofer Heinrich Hertz Institute

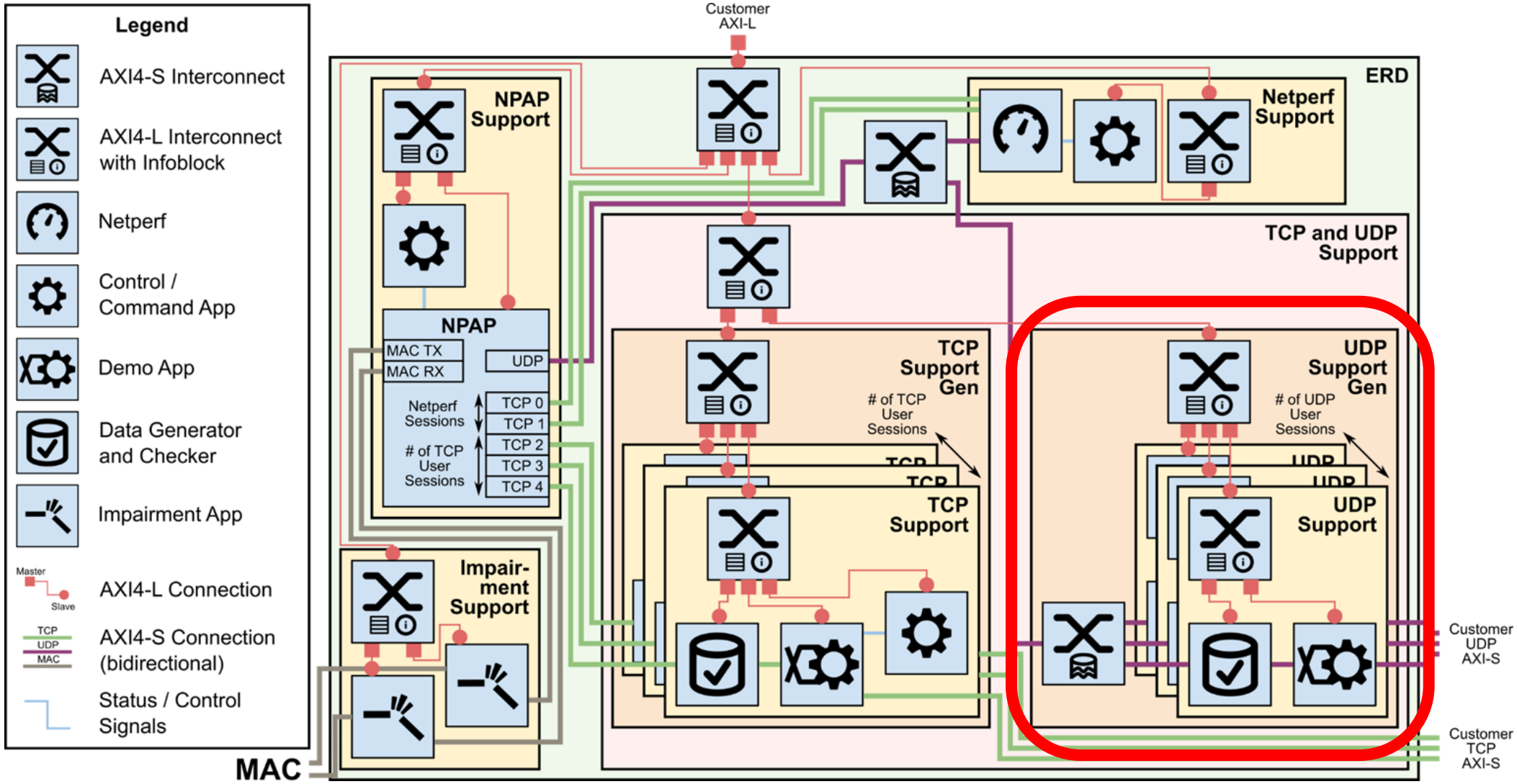
NPAP

Evaluation Reference Design



NPAP

Evaluation Reference Design



NPAP

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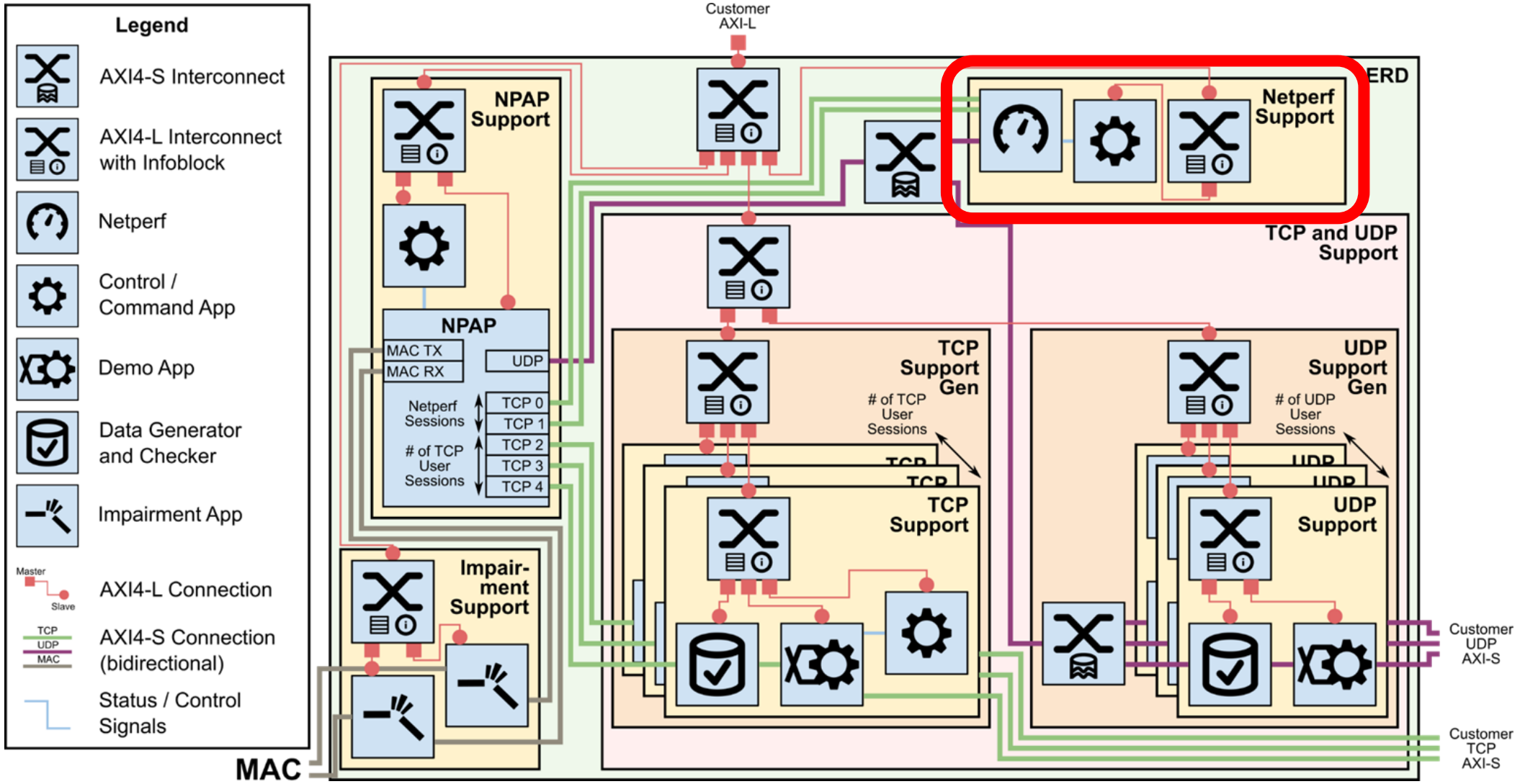
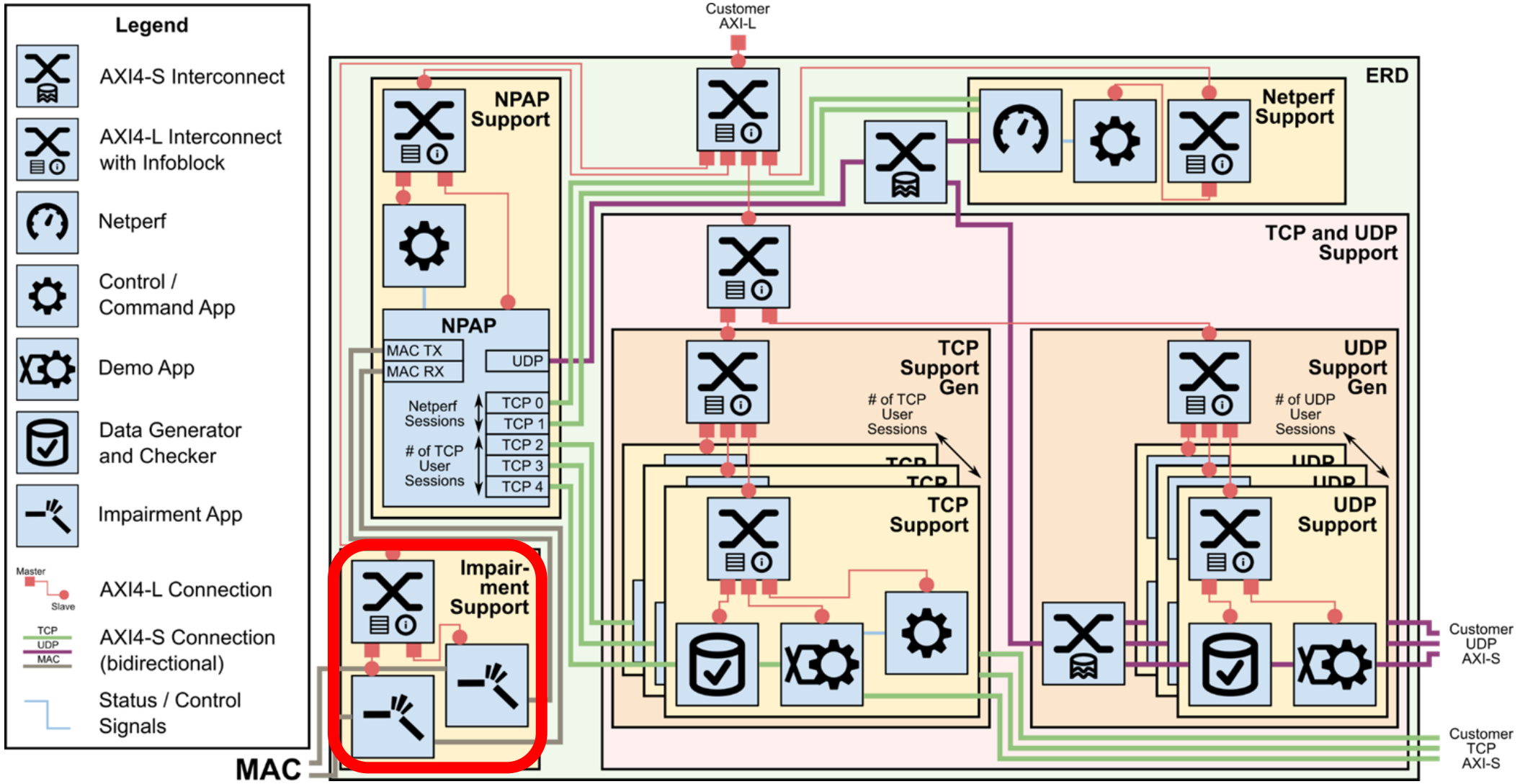


NPAP

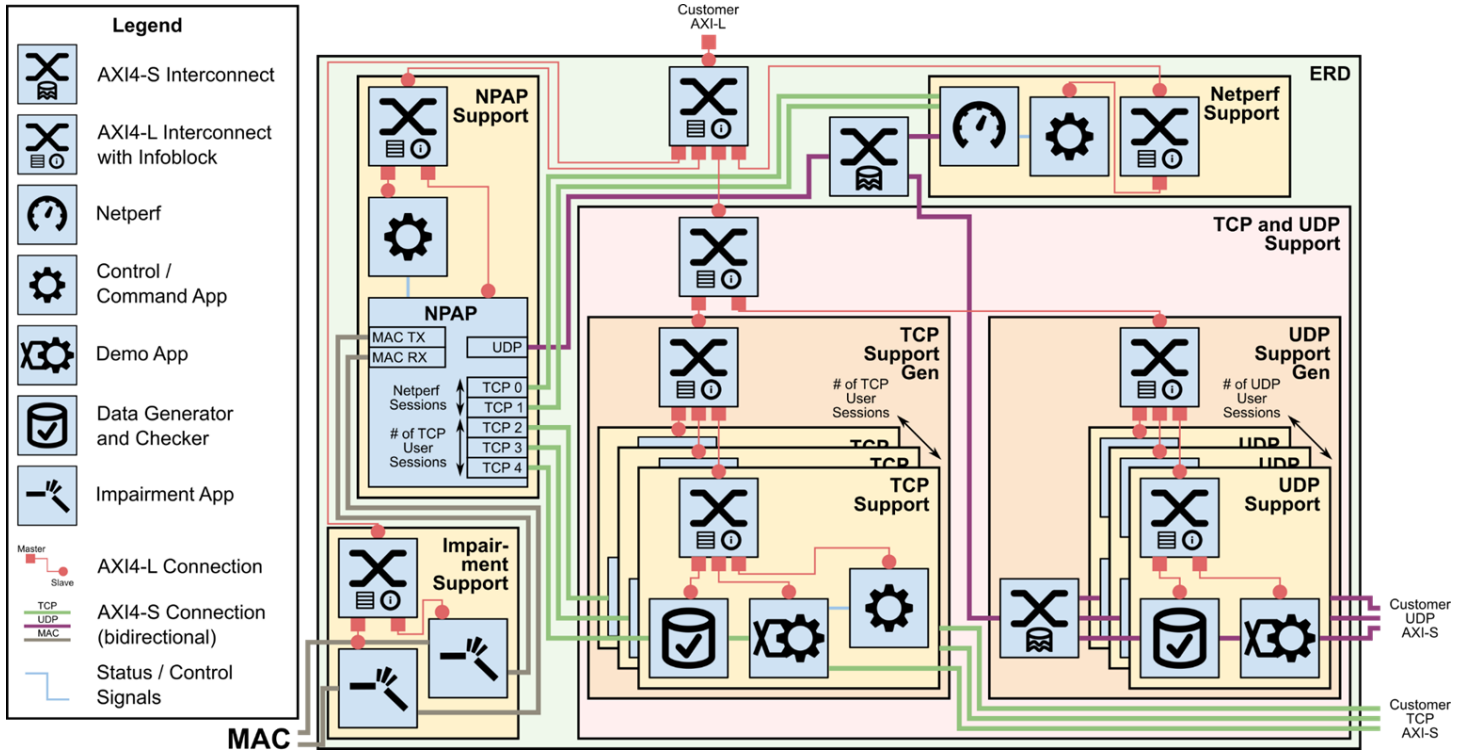
Evaluation Reference Design



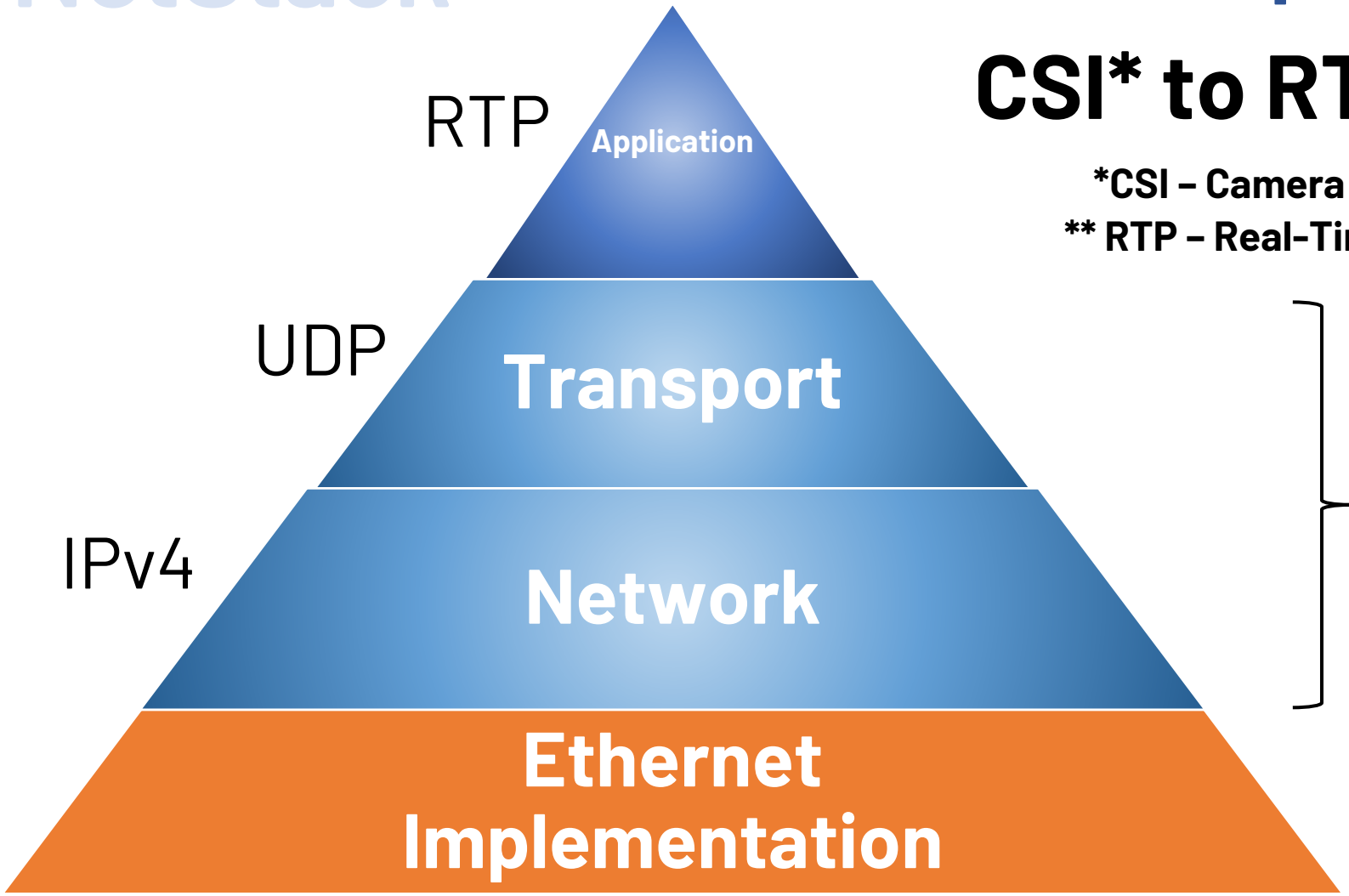
NPAP

Generic Source Code with wide platform coverage

- AMD
  - Virtex 4 to Virtex UltraScale+
  - Kintex to Kintex UltraScale+
  - Artix UltraScale+
  - Zynq-7000
  - Zynq UltraScale+ MPSoC
  - Zynq UltraScale+ RFSoC
  - Versal ACAP Series
- Altera
  - Cyclone IV series
  - Cyclone 10 GX series
  - Stratix V
  - Stratix 10 GX series
  - Agilex 5 D, E Series
  - Agilex 7 F, I, M Series
- Microchip
  - Polarfire and PolarFire SoC
- Lattice
  - Avant-G



RFC-Compliant Implementation



CSI* to RTP** Engine

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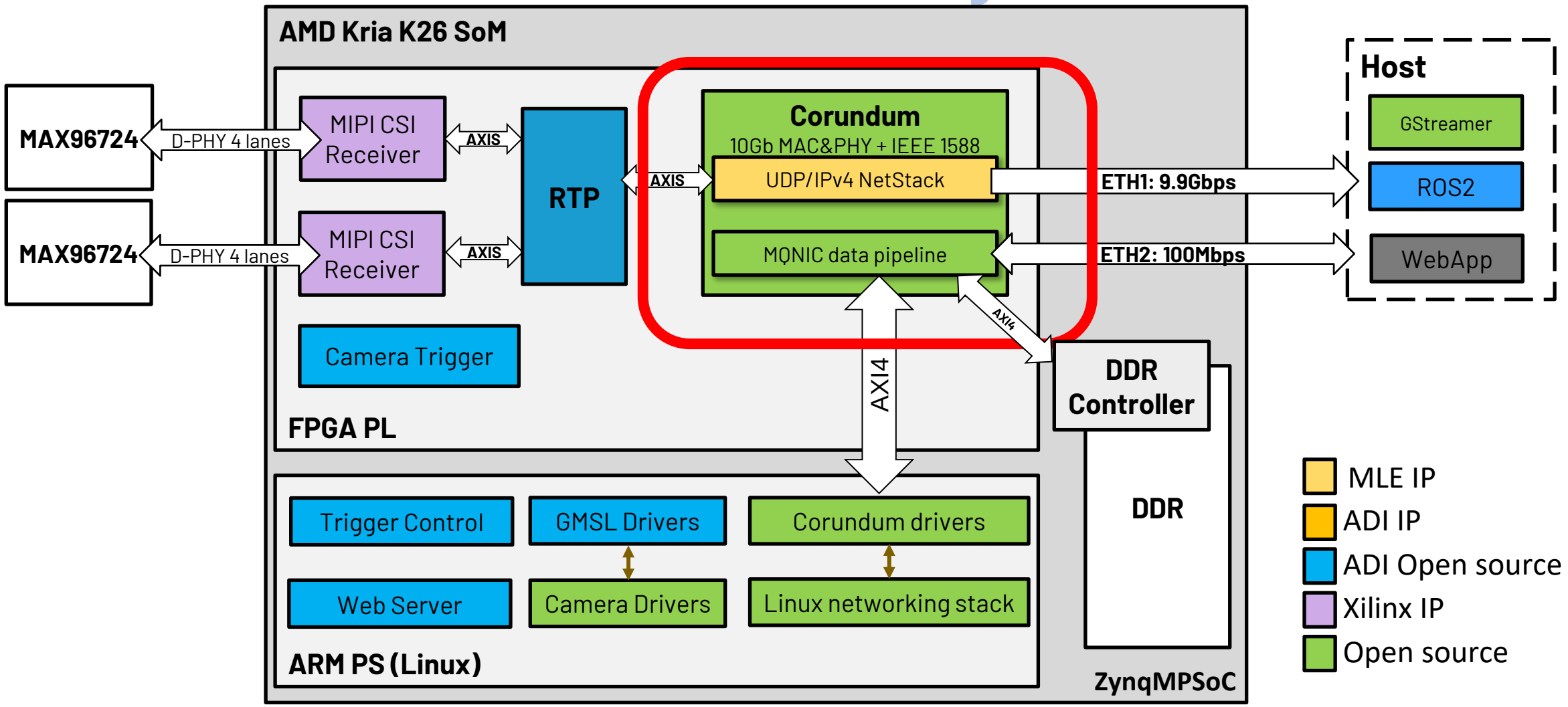
** RTP – Real-Time Transport Protocol

MLE's NPAP

Corundum

Prototype

Overview – Corundum Subsystem

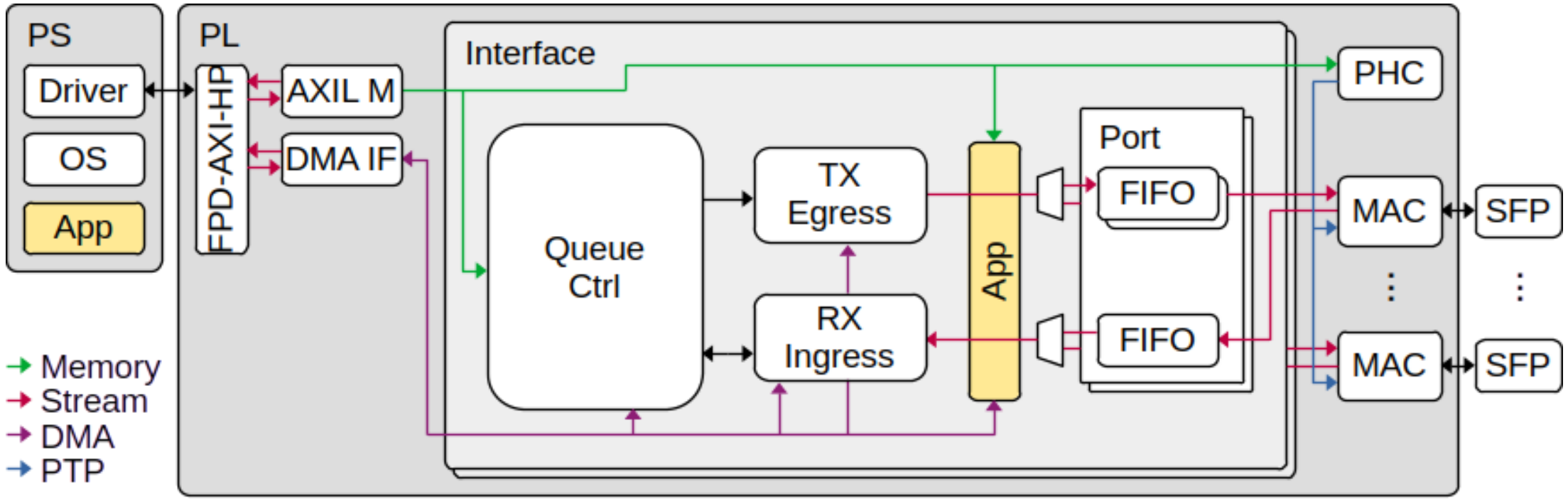


Corundum

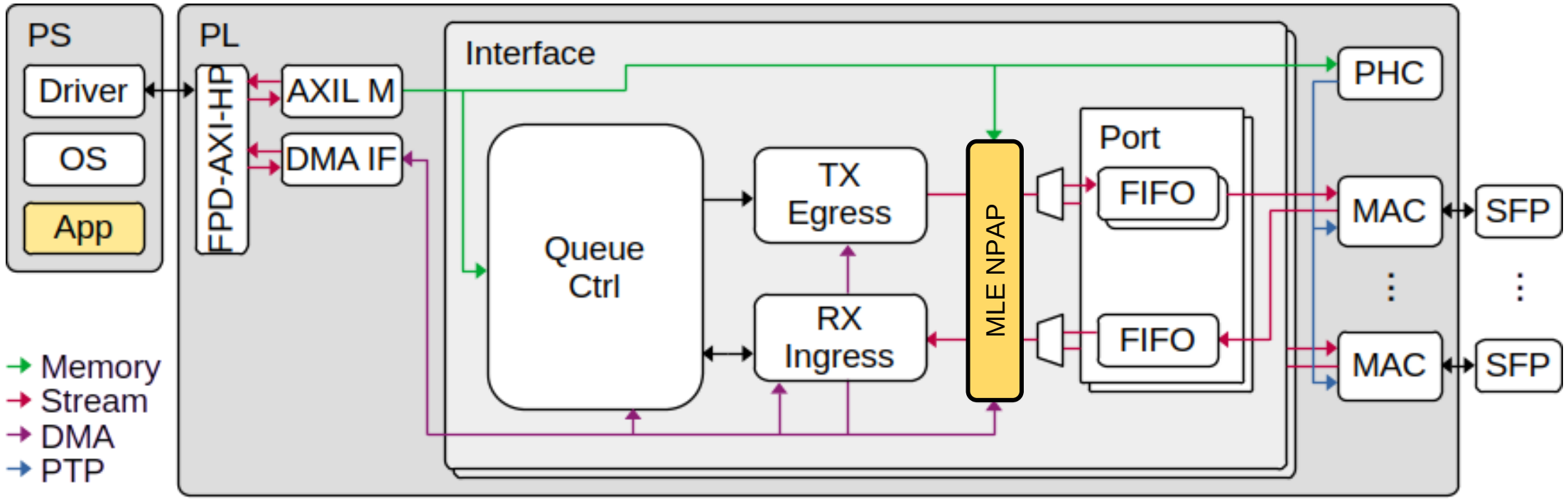
Subsystem – P1

- Open-source, high-performance, FPGA-based NIC
  - PCIe gen 3 x16, multiple 10G/25G/100G Ethernet ports
  - Fully custom, high-performance DMA engine; Linux driver
- Application block for custom logic
- Access to network traffic, DMA engine, on-card RAM, PTP time
- Fine-grained traffic control
- 10,000+ hardware queues, customizable schedulers

Corundum
Subsystem – P2

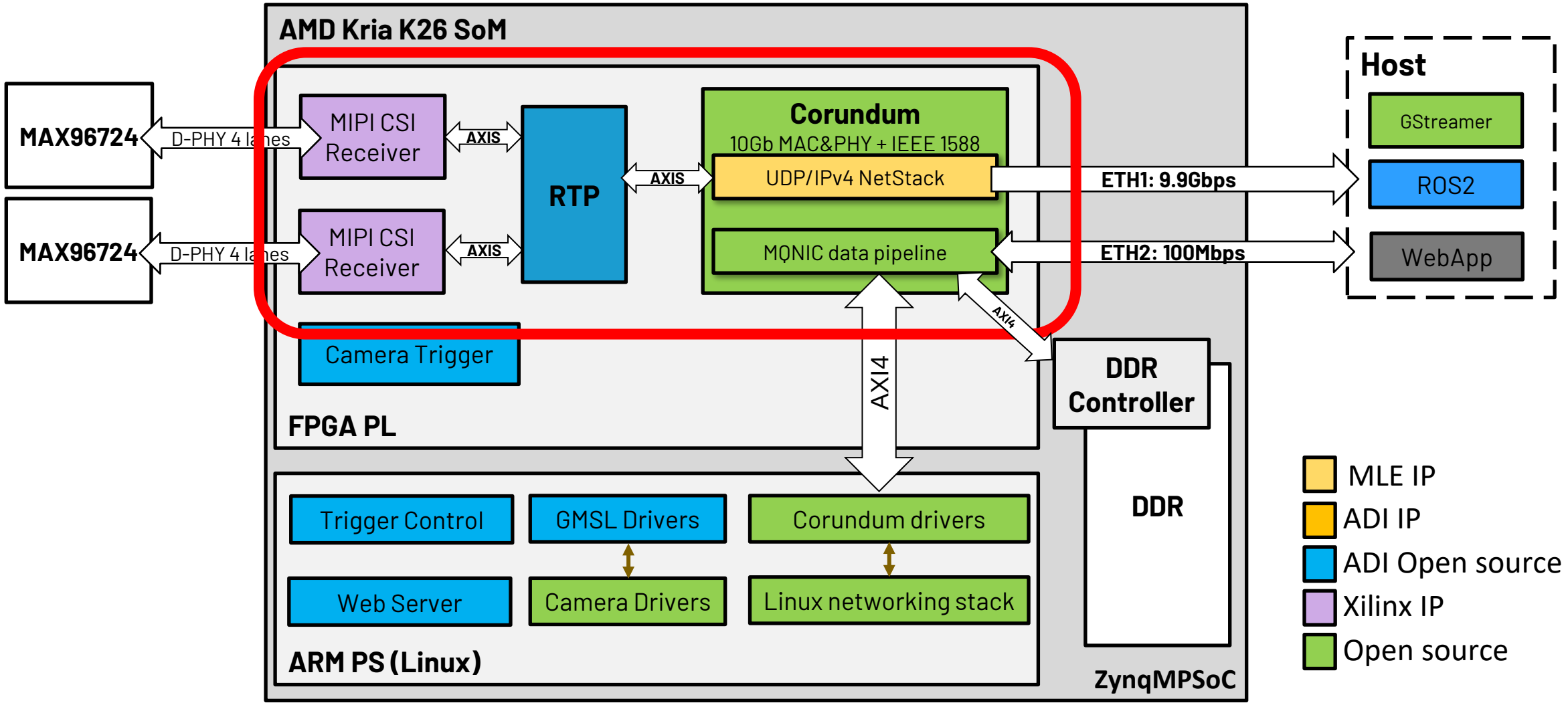


Corundum
Subsystem – P3

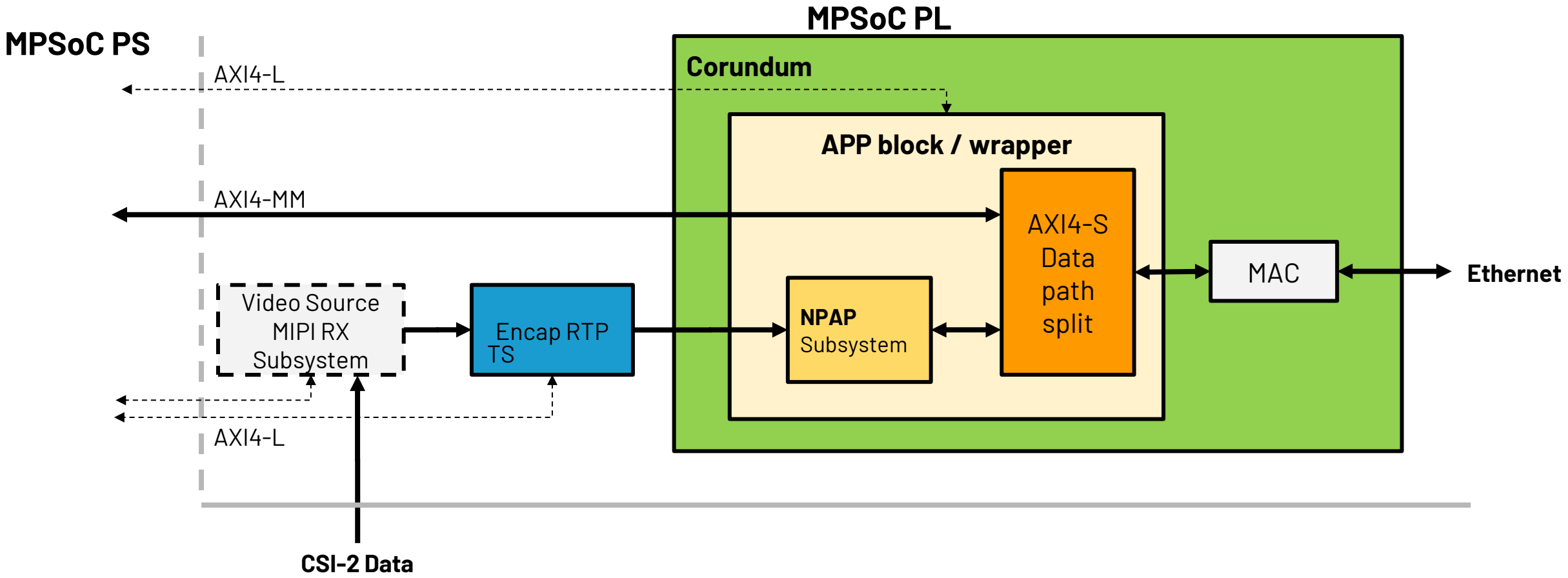


Prototype

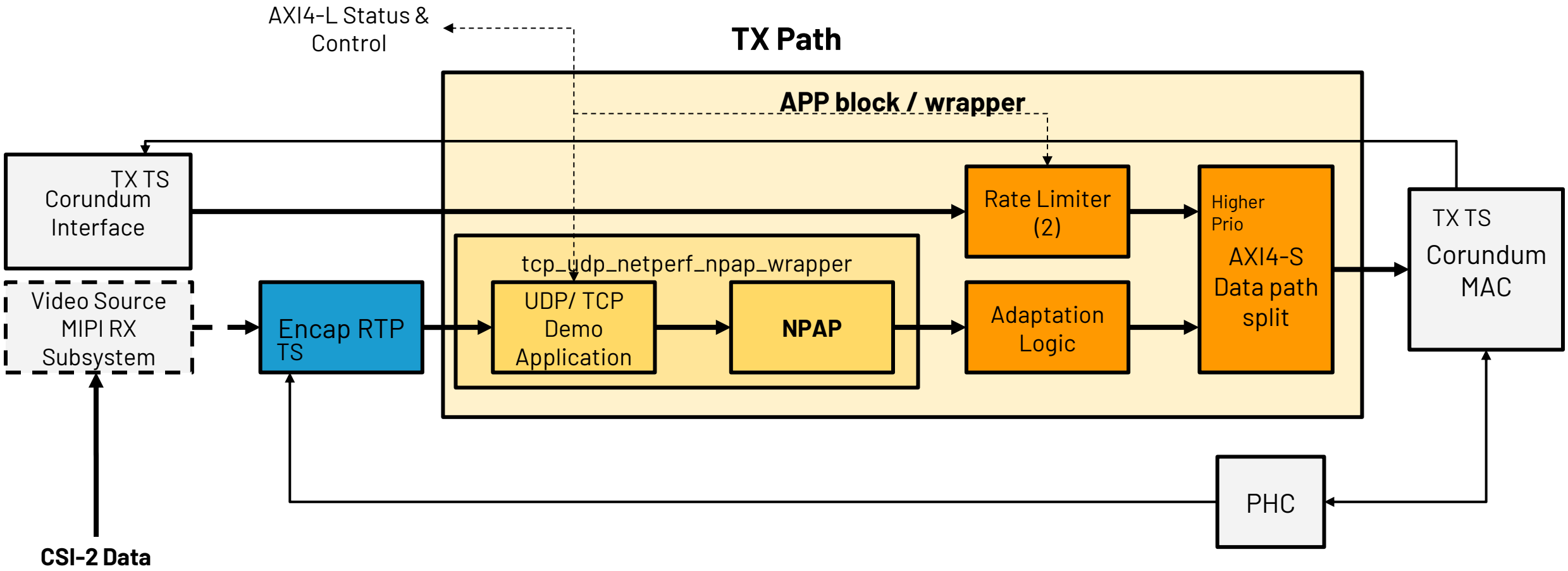
Overview – Corundum and Camera Interface



Corundum and Camera Interface – P1



Corundum and Camera Interface – P2



Hardware Prototype

TierIV GMSL to 10G Ethernet Converter, enabled by ADI

Source: TierIV

Two Quad MAX96724 Deserializers

One 10 GbE-capable SFP+ Connector

Built on top of Xilinx's K26 Industrial-Grade SoM

External Camera Triggering through GPIO header's pins

Prototyped Cameras

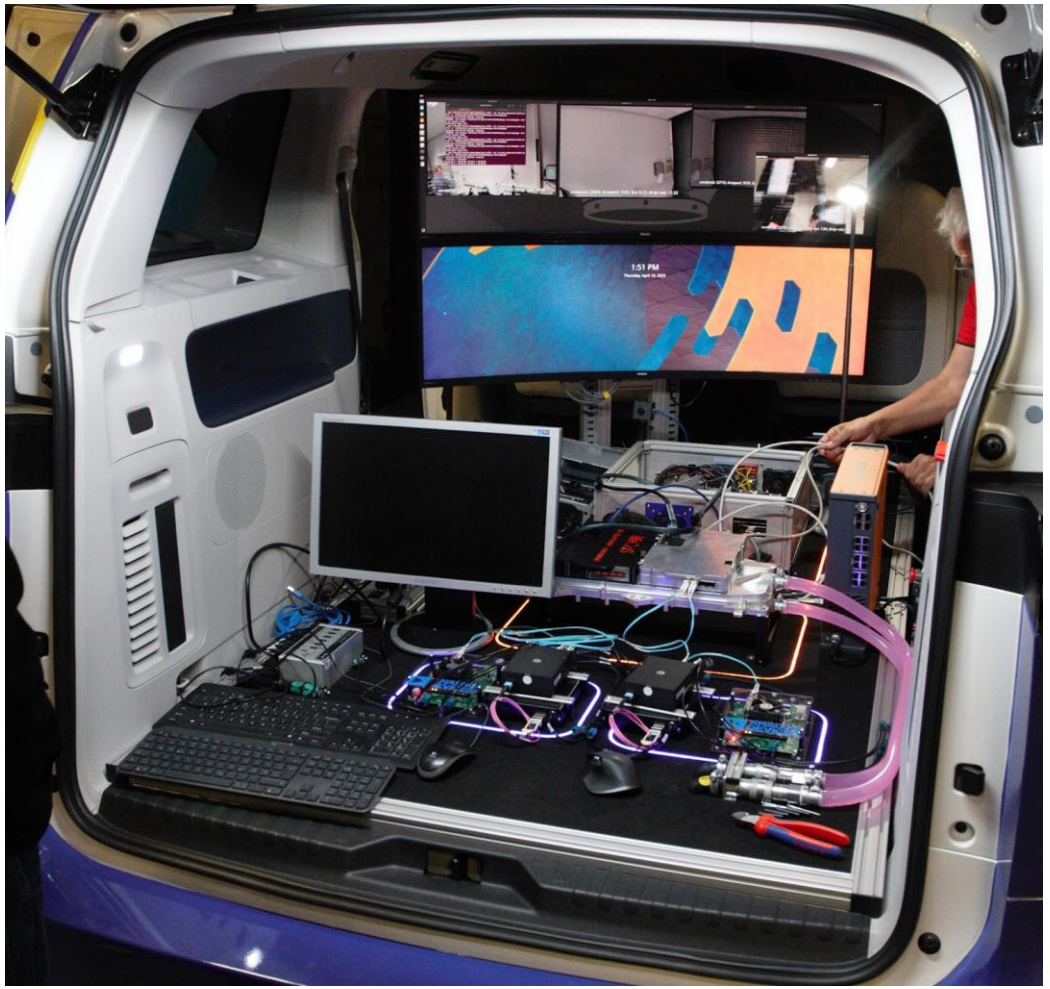
TierIV C1

- 2.5 MP – FullHD+ resolution
- HDR
- Image Sensor + ISP + GMSL2 Serializer
- Output: YUV422

TierIV C2

- 5.4 MP – 2.5K+ resolution
- HDR
- Image Sensor + ISP + GMSL2 Serializer
- Output: YUV422

Prototype
System



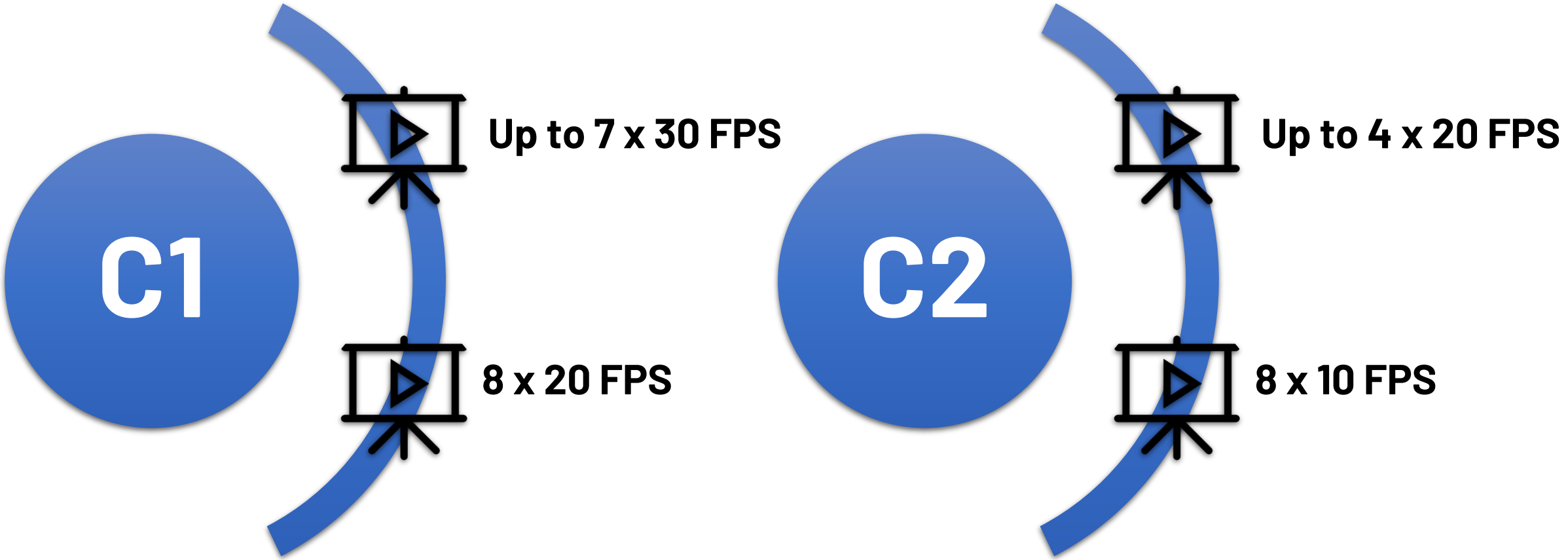
Performance

Traffic Separation

	PC **RX: ~ 9495 Mbps**	**PS** **RX: 135 Mbps**	**PL** **RX: - Mbps**
PC **TX: 135 Mbps**	-	135 Mbps (1x UDP)	-
PS **TX: 95 Mbps**	95 Mbps 1x UDP	-	-
PL **TX: 9400 Mbps**	4x 2350 Mbps 4x UDP	-	-

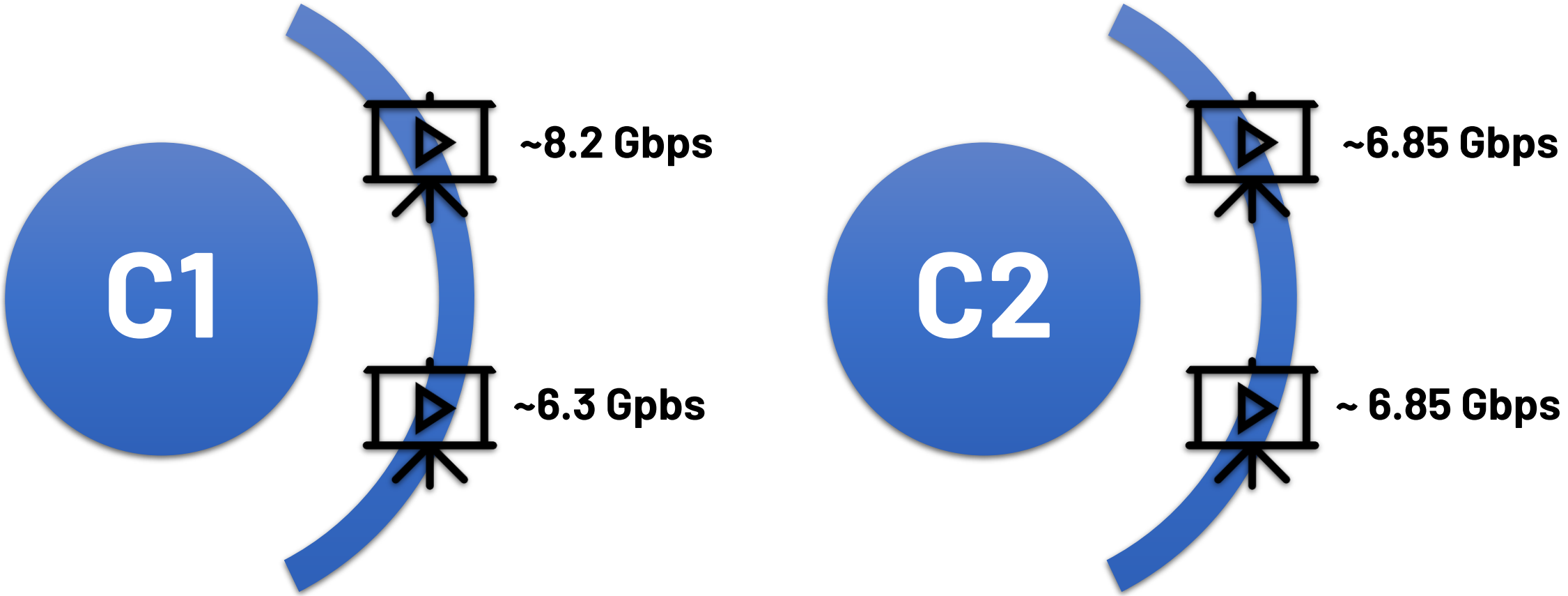
Performance

Overview



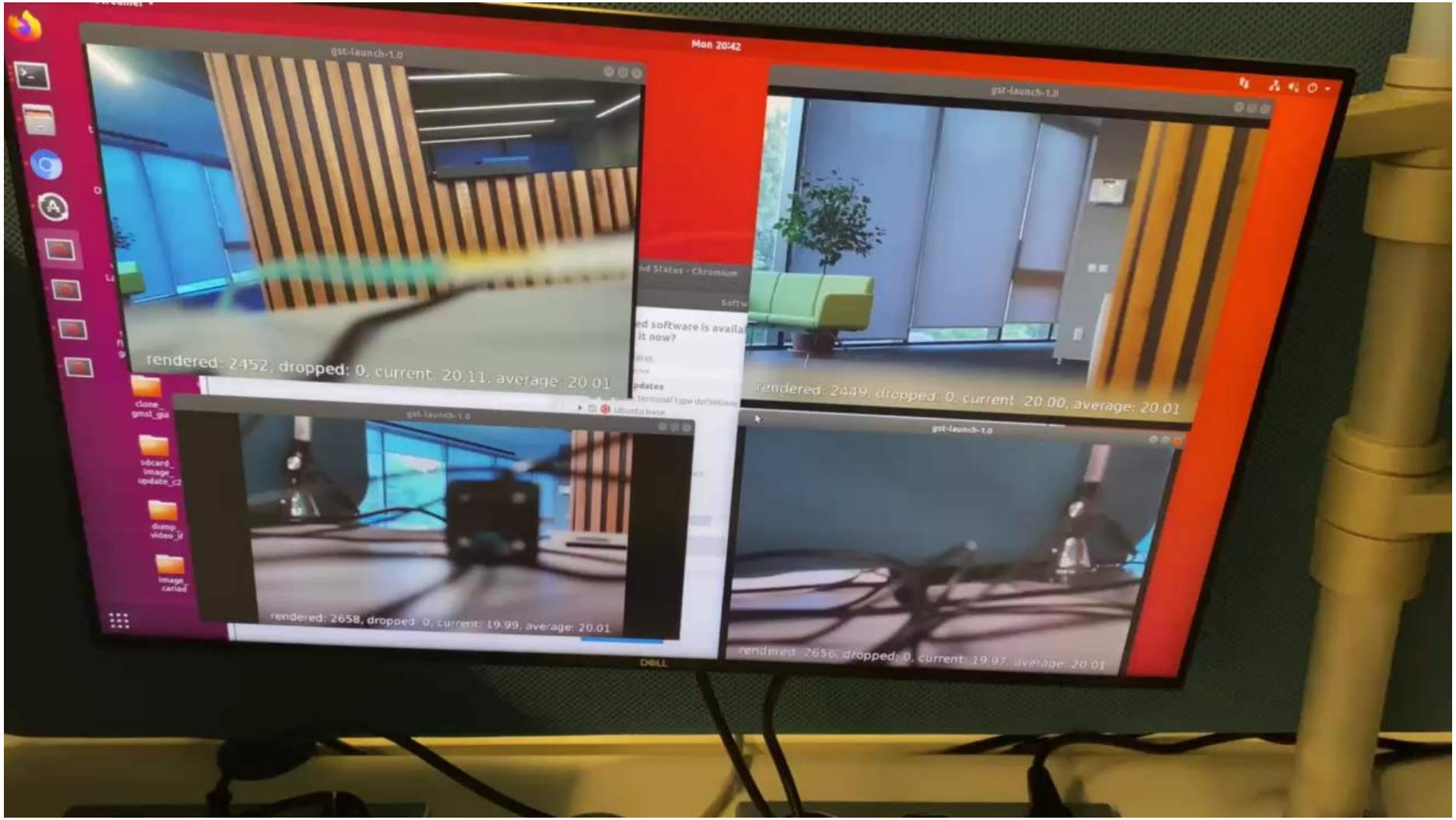
Performance

Overview – in Gbps



Streaming
Demo – C1

Streaming
Demo – C2



Thank You!

Questions?