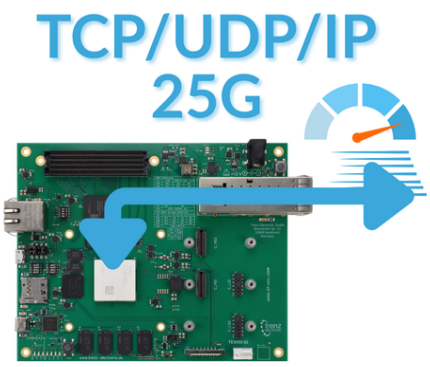
FFSS-TE0950-NPAP-25G Datasheet



The FFSS-TE0950-NPAP-25G is an FPGA Full System Stack (FFSS), i.e. a **customizable FPGA design platform with accelerated 25 GigE network connectivity**.

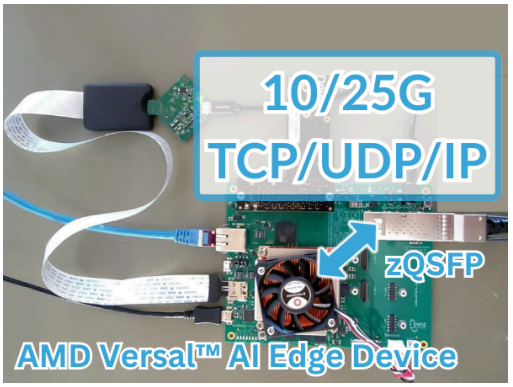
This FFSS combines MLE NPAP (the **TCP/UDP/IP** Network Protocol Acceleration Platform) with Trenz Electronic's **TE0950** Evaluation Board featuring the **AMD Versal™ AI Edge VE2302**.

All key functionality is pre-integrated and pre-validated and ships as a **compilable FPGA design project** along **with an IP-Core license** from MLE.

Use Cases

Application development of high data-rate networked systems[1] where **Your FPGA logic** transmits and/or receives data over a TCP/UDP/IPv4 network at speeds up to 25 Gbps line-rate. Examples include:

- High-resolution Radar/Lidar/Camera sensor nodes
- Robotics control
- ADAS sensor frontends
- High-speed Data Acquisition



Implement Your sensor and/or actuator frontend inside Programmable Logic and connect via bi-directional 128 bit wide AXI4-Stream on-chip interfaces with MLE's NPAP to transmit and/or receive Your data over TCP/UDP/IP over 25 GigE via the zQSFP of the TE0950 board.

FPGA Full System Stack Key Features

- 150k LUTs total (approx. 120k LUTs free-for-use and 30k LUTs reserved by FFSS)
- Trenz TE0950 (AMD Versal™ AI Edge XCVE2302-1LSESFVA784 SoC with 8 GByte DDR4 SDRAM)
- 25 GigE subsystem, configured and wired to zQFSP via AMD PG292 and via MLE NPAP-25G
  - 1x TCP port (interoperable with Linux, Microsoft Windows, SolarFlare, Mellanox TCP/IPv4)
  - 1x UDP port (interoperable with Linux, Microsoft Windows, SolarFlare, Mellanox UDP/IPv4)
  - PL-based Data Generator and Data Checker test application (use as design example)
- Linux OS (pre-installed root filesystem on SDCard)
- 1x RJ45 1 GigE LAN port (fully accessible from Linux)

Ordering Information

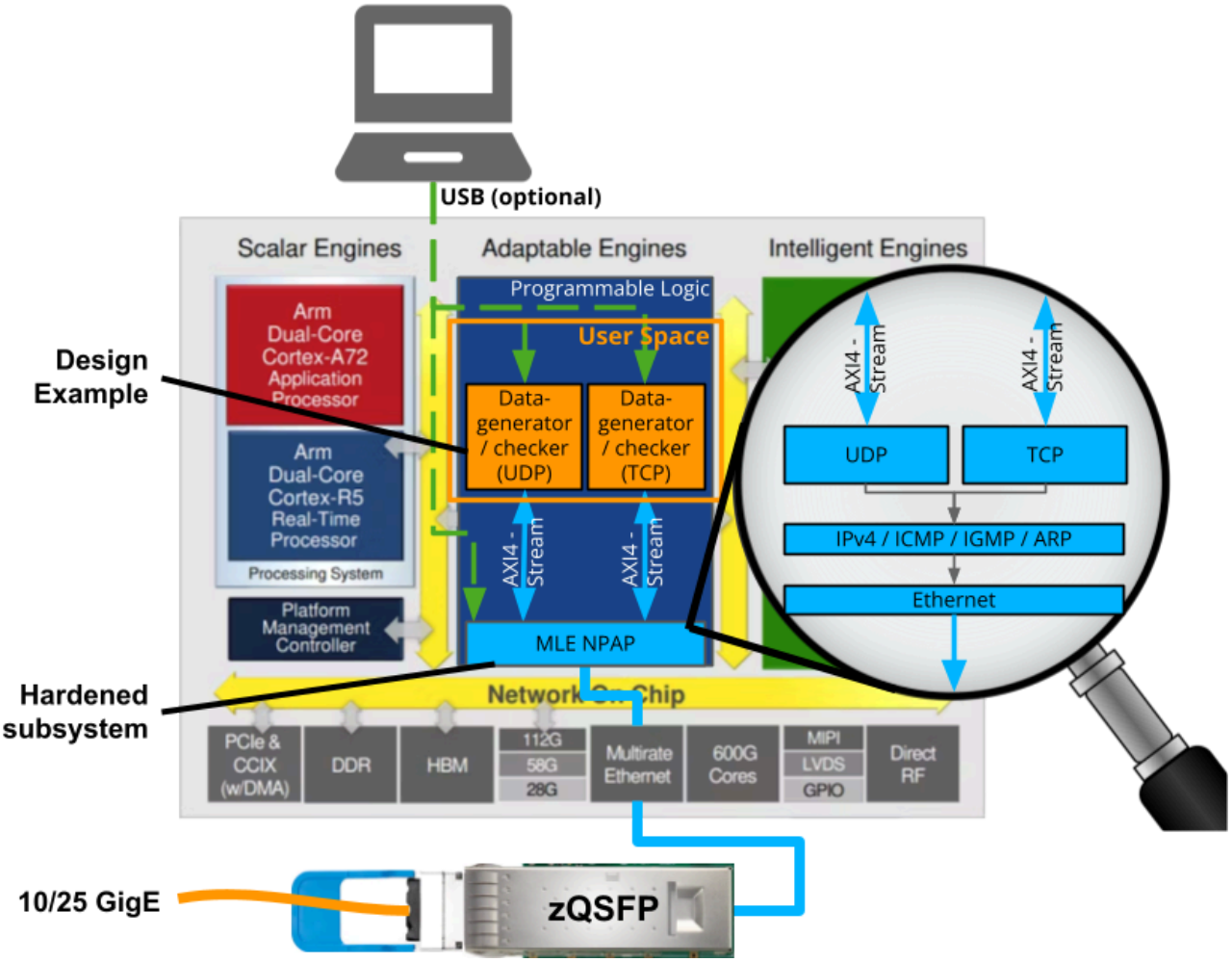
Model Name	Part Number	Description
TE0950 with Full Accelerated 25G TCP/UDP/IP	FFSS-TE0950-NPAP-25G-01	Accelerated TCP/UDP/IP networking in PL up to 25 Gbps linerate, based on TE0950

[1] This product is not designed or intended to be fail-safe, or for use in any application requiring fail-safe performance.

FFSS Software and System-Level Block Diagram

This FFSS builds on top of the AMD Versal™ AI Edge XCVE2302 SoC[2] on the Trenz Electronic's TE0950 board[3] and runs open-source Linux. The 25 GigE subsystem is fully configured and wired to zQFSP via AMD PG292[4] and via MLE NPAP-25G[5] TCP/UDP/IP Network Protocol accelerator.

For each, TCP and UDP, a Data Generator and Data Checker test application has been implemented inside the FPGA programmable logic. Besides testing and performance benchmarking this test application can be used as an example for integrating Your FPGA logic!

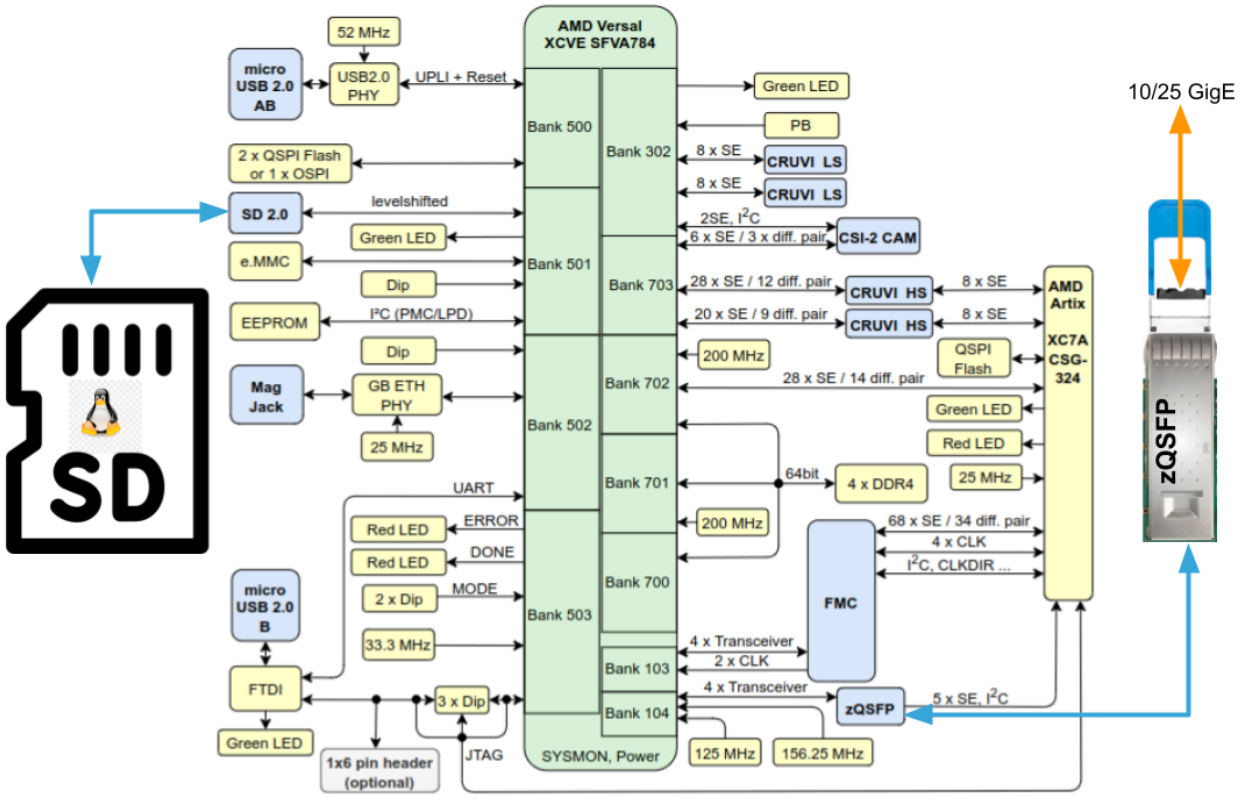


Simply connect the TE0950 to your network and a PC via UART to immediately control and validate the 25G connection using the provided software. For custom hardware development, you can connect your own logic directly to the well-documented AXI4-Stream data interfaces to begin sending and/or receiving TCP and/or UDP data.

[2] https://www.amd.com/en/products/adaptive-socs-and-fpgas/versal/ai-edge-series.html
[3] https://www.trenz-electronic.de/en/AMD-Versal-AI-Edge-Evalboard-with-VE2302-device-8-GB-DDR4-SDRAM-15-x12-cm/TE0950-03-EGBE21C
[4] https://docs.amd.com/r/en-US/pg292-ethernet-1-10-25g
[5] https://www.missinglinkelectronics.com/ip-cores/npap-tcp-udp-ip-stack/

FFSS Hardware Block Diagram

The hardware foundation for this FFSS is Trenz Electronic's TE0950 Evalboard featuring the AMD Versal™ AI Edge XCVE2302 SoC connected to many external I/Os.



- AMD Versal™ AI Edge XCVE2302-1LSESFVA784 device
  - A784 package (pin compatible VE2202, VE2302, VM1102)
  - AMD Artix™ 7 FPGA as configurable Levelshifter/MUX for FMC and other 3.3 V IOs
- 8 GByte DDR4 SDRAM
- 128 MByte QSPI Flash (primary boot option)
- MicroSD card (primary boot option)
- 32 GByte eMMC (secondary boot option)
- USB 2.0 Host/Device/OTG (type Micro A/B connector)
- Gigabit Ethernet RJ45
- zQSFP with 4 GTYP Transceiver
- 2 x CRUVI HS
- 2 x CRUVI LS
- CSI-2 connector (camera, 2 lane MIPI)
- FMC: 4 GTYP Transceiver
- Dimension: 150 mm x 120 mm
- More details at [Trenz TE0950 Wiki]

Deliverables

- 1x Trenz TE0950 board
- 1x power adapter
- 1x CoolJag BUF-A4 Fansink
- 1x SD Card (to install root file system)
- Full FPGA System Stack including Software, Firmware, Gateware (i.e. SD Card image with bitfile, Board Support Package, Linux, drivers. Downloadable as binaries and in the form of FPGA Design Project Archive (compilable netlist).
- Single-project-use fully paid-up-for, perpetual commercial license for single unit (See license details below)

Licensing

This FFSS comprises the following licenses from MLE. For more information regarding the legal license please refer to https://missinglinkelectronics.com/de-license

Proof-of-License (example)
Licensee: *<YOU / YOUR COMPANY>*
Product: "NPAP-25G-SPNL" (NPAP-25G Single-Project-Use Netlist License)
Project: *<YOUR PROJECT NAME>*
License Term: Perpetual
License Type: Fully-Paid-Up-For, Worldwide, Commercial Single-Project-Use License
Designated Equipment: AMD Versal™ AI Edge XCVE2302-1LSESFVA784 on TE0950
Designated Number of Instantiations: 1 (One)
Designated Number of Units: 1 (One)
Designated Site: *<YOUR COMPANY ADDRESS>*

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FPGA Full System Stack (FFSS)

"When Wall Street wanted to program computers without having computer programmers, they invented the spreadsheet!" - This was our spirit when we came up with the FPGA Full System Stack: Make building FPGA-based systems easier for engineers without expert knowledge in FPGA design.

Why FPGA Full System Stack?

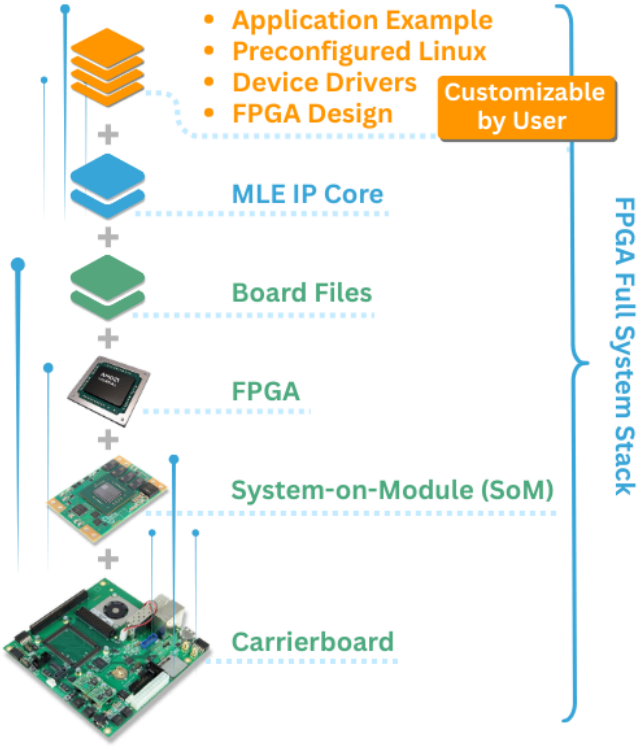
For compute-intensive, time-critical applications in Automotive, Aerospace/Defence, Industrial/Scientific/Medical, FPGAs are often the choice. However, programming FPGAs, particularly those System-on-Chip (SoC) FPGA with embedded CPUs, has long been considered complex and risky.

Integrated and pre-validated building blocks of FPGA hardware and software subsystems, which we call "FPGA Full System Stack" can greatly de-risk development and accelerate new product initiatives.

What makes up the FPGA Full System Stack?

Every FPGA Full System Stack comprises the following elements (top-down):

1. Application Example Subsystems which are customizable by users based on your applications
2. A Targeted Performance Subsystem, including one or more MLE IP-Cores
3. A Board Support Package, with a Linux Base System and Board Part Files
4. The FPGA device (such as the AMD VE2302, for example)
5. A SoM (such as the TE0955, for example)
6. A carrierboard (such as TEBF0955, for example)



Pre-integrating and testing this complex stack gives you, the implementer the advantages:

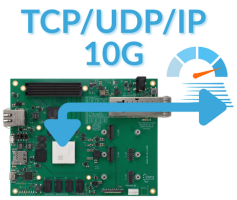
1. You can rely on a tested and verified subsystem implementation. The concept of re-use increases design productivity while sharing the FPGA subsystem development costs and risks over many users.
2. Pre-validated FPGA IPs and Subsystems make clever use of different FPGA resources to realize a cost/performance optimized domain-specific architecture. No need for reading long datasheets or making timing closure.
3. Operating system and application software is included in the form of kernel space device drivers, user-space programmer APIs, and sometimes even complete OS images, all nicely tuned for guaranteeing the overall system's reliability and performance.

Other FPGA Full System Stacks

MLE and Trenz Electronics have been planning for many different FFSS to come. Our initial focus is on "embedded" platforms for performance networking and for performance storage / data acquisition based on AMD Versal AI Edge. Below are some examples.

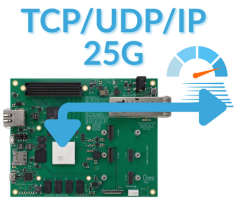
If you are interested in other boards, other FPGA devices or other functionality, please contact us!

Network Acceleration



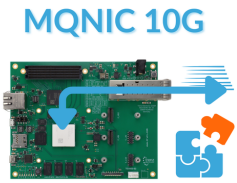
FFSS-TE0950-NPAP-10G

Accelerated TCP/UDP/IP networking in PL up to 10 Gbps linerate, based on TE0950



FFSS-TE0950-NPAP-25G

Accelerated TCP/UDP/IP networking in PL up to 25 Gbps linerate, based on TE0950

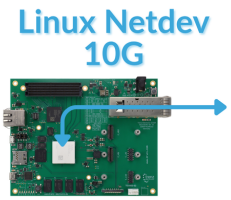


FFSS-TE0950-MQNIC-10G

A configurable Multi-Queue FPGA NIC for 10 GigE in-network processing, based on TE0950

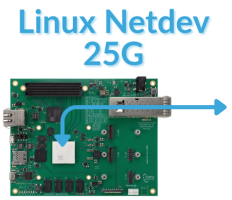
FFSS-TE0950-MQNIC-25G

A configurable Multi-Queue FPGA NIC for 25 GigE in-network processing, based on TE0950



FFSS-TE0950-Netdev-10G

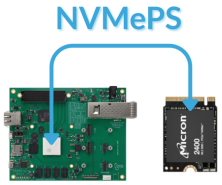
ARM A72 Linux 10 GigE NIC with a complete network stack (non-accelerated), based on TE0950



FFSS-TE0950-Netdev-25G

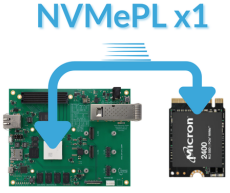
ARM A72 Linux 25 GigE NIC with a complete network stack (non-accelerated), based on TE0950

Storage Acceleration



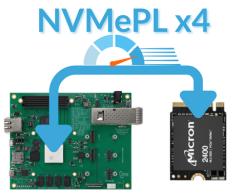
FFSS-TE0950-NVMePS

Data read/write onto a Linux-connected NVMe SSD using Linux file system, based on TE0950



FFSS-TE0950-NVMePL-x1

Accelerated NVMe data streaming with 1 lane in PL, based on TE0950



FFSS-TE0950-NVMePL-x4

Accelerated NVMe data streaming with 4 lanes in PL, based on TE0950