100G TCP/UDP/IPv4 Accelerators for AMD Alveo

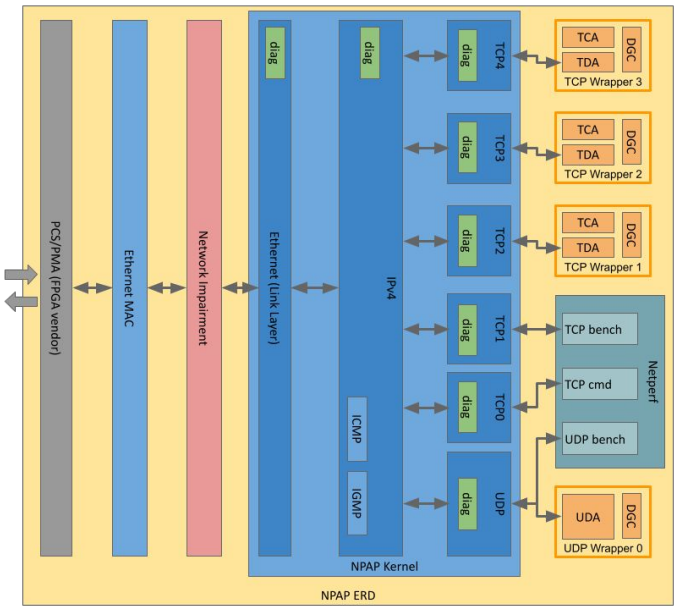
MLE has optimized for AMD Alveo FPGA Cards the industry proven TCP/UDP/IPv4 Network Protocol Acceleration Platform (NPAP). Originally developed by Fraunhofer HHI, NPAP implements fast and reliable networking solutions for high-bandwidth, low-latency Multi- Gigabit Ethernet.

Application Use Cases

- Full TCP/UDP/IPv4 connectivity
- High-speed sensor DAQ: Stream data from FPGA into Network-Attached Storage (NAS)
- High-speed robotics control: Stream data from servers via FPGA into actuators
- High-bandwidth, low-latency automotive ECU-to-ECU connectivity e.g. for SOME/IP
- SmartNIC using TCP/IPv4 “Full Acceleration”
- Hyper-converged storage acceleration, for “over-Fabric” NVMe/TCP
- Computational Storage Processing (CSP) with NVME via PCIe Peer-to-Peer

Accelerator System Architecture

- 50+ dedicated TCP Cores
- Single UDP Core
- Netperf Bandwidth, Latency Benchmark
- Network Impairment / BERT (optional)
- Network Diagnostics (optional)



Key Features

- Highly modular TCP/UDP/IPv4 Stack implementation for MAC, Ethernet, IPv4, TCP, UDP processing implemented in synthesizable HDL
- IPv4 with ICMP and IGMP
- Bi-directional 128-bit data streams to deliver line rates up to 80 Gbps (depends on FPGA speed)
- Multiple, parallel TCP engines (sockets) for predictable scalable processing
- Network Interface Card (NIC) with optional Bypass and PCIe DMA
- Point-to-point of LAN capable
- User applications for payload processing either in programmable logic or in software via PL/PS datamovers
- Resource analysis for full stack including UDP plus 2 TCP ~30k LUTs, +10k LUTs for each additional TCP engine

License Models and Availability

- As IP Core or customized FPGA subsystem
- Single-Project-Use Netlist (or equiv.)
- Multi-Project-Use Source Code
- Customized, integrated turnkey solutions
- Application-specific expert design services

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Runs on AMD Alveo FPGA Accelerators

- Full network stack with support for U50, U55C, U200, U250, U280, V80, V80-LL
- TCP/UDP Netperf/Netserv - interops w/ open-source Netperf/Netserv V2.6
- TCP Loopback and UDP Loopback
- Stack control software (for IPv4 addresses, diagnostics and statistics, etc)
- Complete reference design with Ethernet, ICMP, IGMP, IPv4, UDP, TCP and PCIe DMA
- 25/50/100 GigE with up to 60 Gbps linerate per single TCP Session
  Integrated with AMD/Xilinx 10G/25G Ethernet Subsystem PG210 and GTH transceivers
- 100 GigE with up to 78 Gbps linerate
  Integrated with Xilinx Ultrascale Integrated 100G Ethernet Subsystem PG165 (CMAC)
- QSFP28 for 100 GigE via Twinax or Fibre

Fraunhofer Heinrich-Hertz-Institute (HHI)

Founded in 1949, the German Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. With a workforce of over 23,000, the Fraunhofer-Gesellschaft is Europe's biggest organization for applied research, and currently operates a total of 67 institutes and research units. The organization's core task is to carry out research of practical utility in close cooperation with its customers from industry and the public sector.

Fraunhofer HHI was founded in 1928 and joined in 2003 the Fraunhofer-Gesellschaft as the "Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut„ Today it is the leading research institute for networking and telecommunications technology, "Driving the Gigabit Society" .

Missing Link Electronics (MLE)

We are a Silicon Valley based technology company with offices in Germany. We are partner of leading electronic device and solution providers and have been enabling key innovators in the automotive, industrial, test & measurement markets to build better Embedded Systems, faster.

Our mission is to develop and market technology solutions for Embedded Systems Realization via pre-validated IP and expert application support, and to combine off-the-shelf FPGA devices with Open-Source Software for dependable, configurable Embedded System platforms.

Our expertise is Domain-Specific Architectures I/O connectivity and acceleration of data communication protocols, additionally opening up FPGA technology for analog applications, and the integration and optimization of Open Source Linux and Android software stacks on modern extensible processing architectures.

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