Cost-Optimizing High-Accuracy Precision Time Protocol

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Missing Link Electronics

MLE – Experts for Domain-Specific Compute Architectures

Our Mission: From Software to Silicon!

- Deliver HW and SW for High-Performance (Embedded) Compute Systems & Solutions
- Offering pre-validated subsystems with FPGA IP blocks and open-source software
- Support customer projects with deep expertise and hands-on design services

AMD Adaptive Computing Partner PREMIER

trenz electronic GmbH

Head-quartered in Silicon Valley with Design Offices in Germany

- Founded 2010
- 20+ Certified FPGA Designers
- Customers include technology leaders, US and European government agencies, Fortune 500 companies
- Partners to:

PCI SIG

Fraunhofer IPMS

ulm university universität uulm

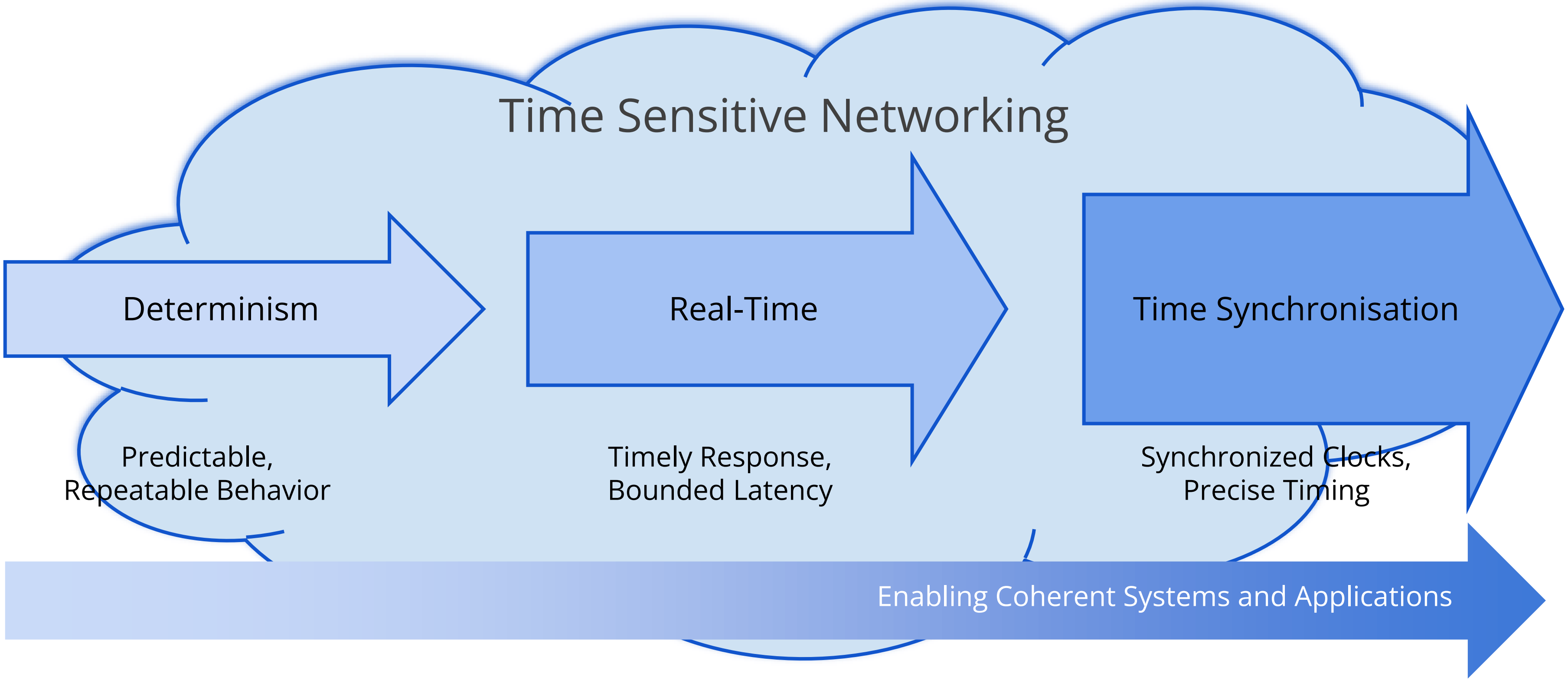
THU Technische Hochschule Ulm

BHT Berliner Hochschule für Technik

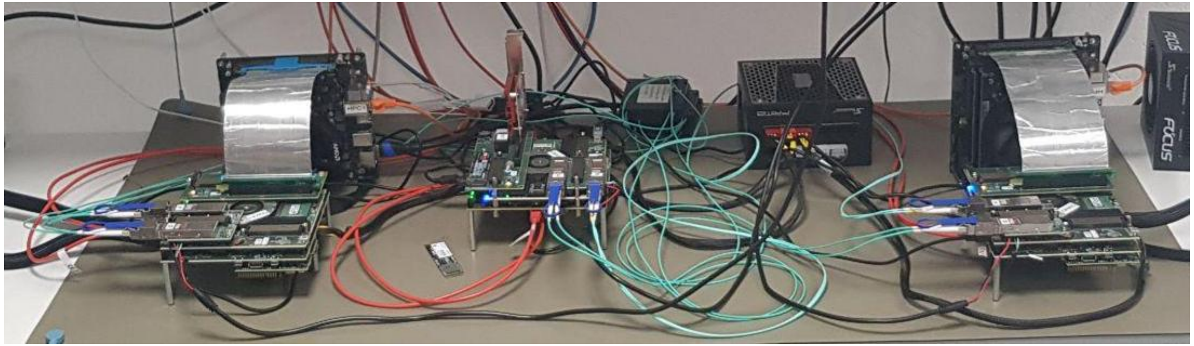
ELEMASTER

Fraunhofer Heinrich-Hertz-Institut

TSN: From Determinism to Time Synchronisation



1 GbE TSN gPTP



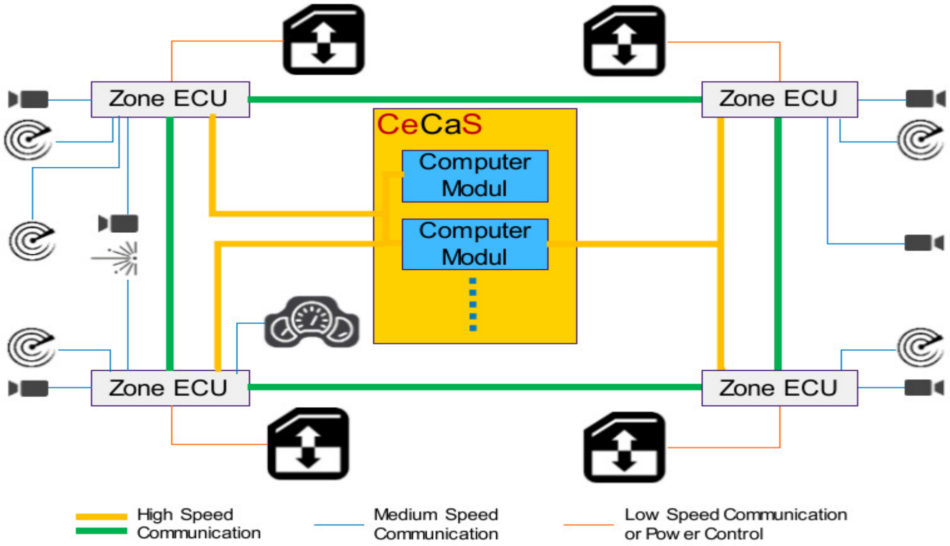
Not optimized Labcar (2020)

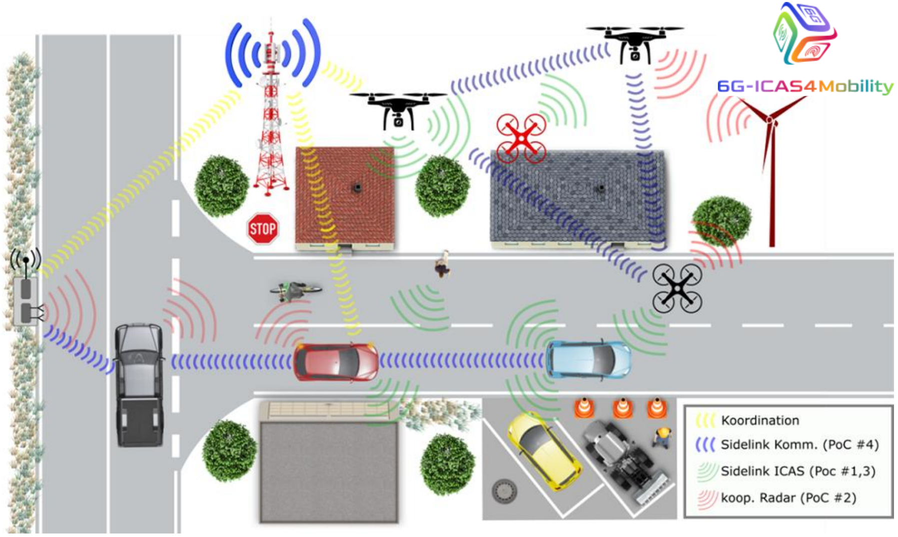
PPS stddev	?
PPS Range	< 110 ns
PPS Avg	< 30 ns
Measurements	?

Research Projects

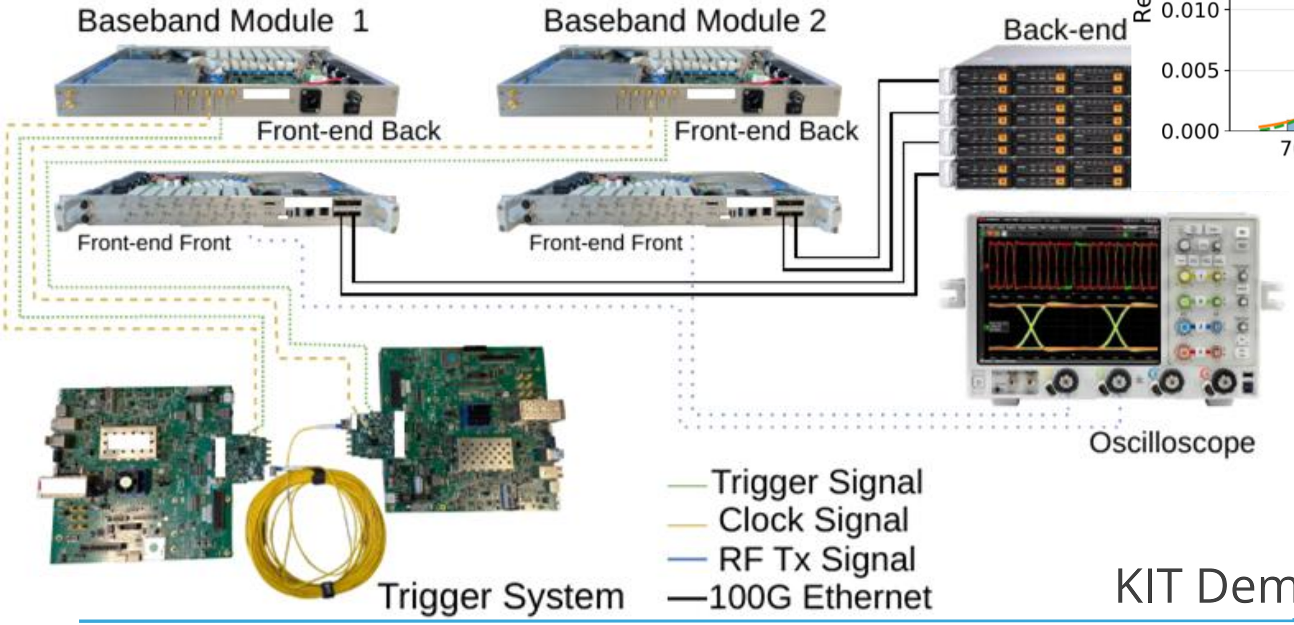
With funding from the:

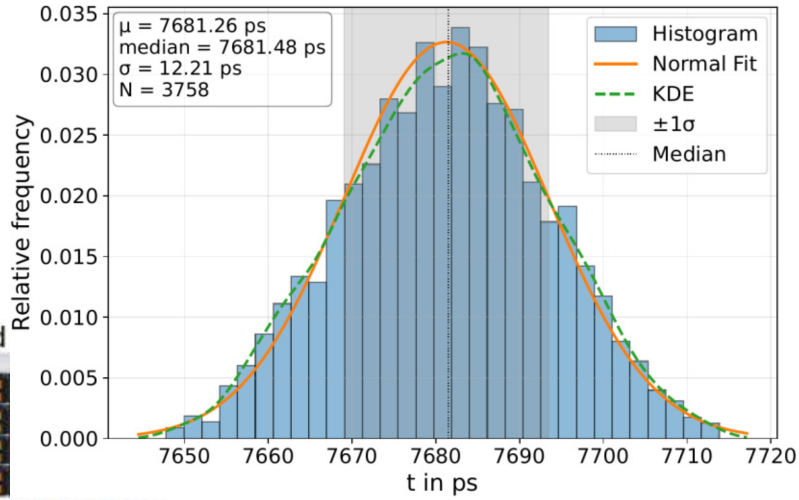
Federal Ministry
of Research, Technology
and Space





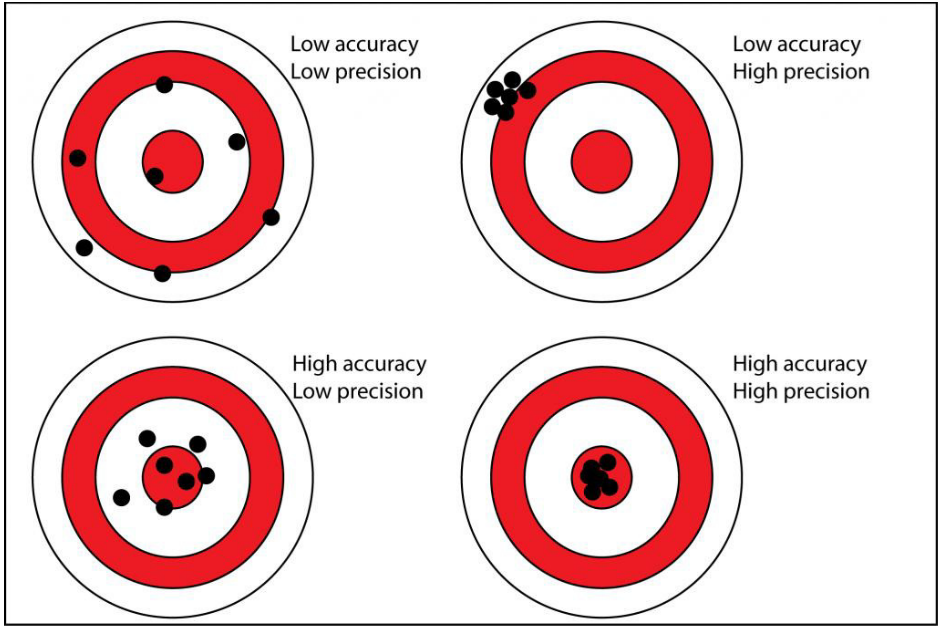
VERANO OFDM MIMO Demo



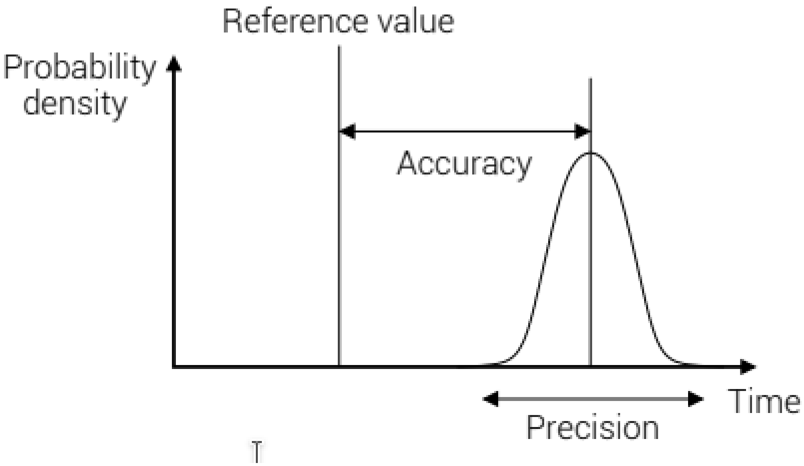


KIT Demonstrator & Measurement

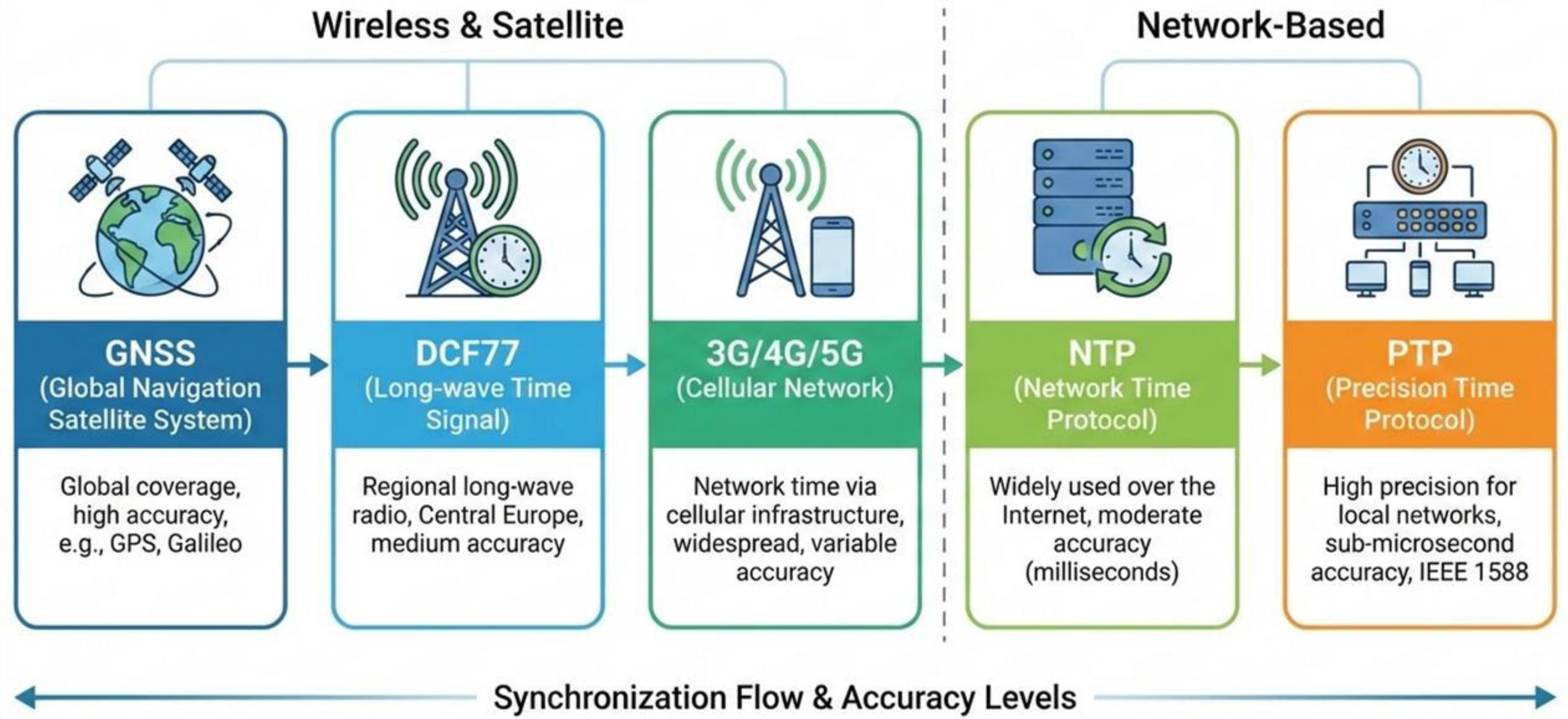
Refresher: Accuracy vs. Precision



https://www.portaspecs.com/precision-and-accuracy/



Time Synchronization Options

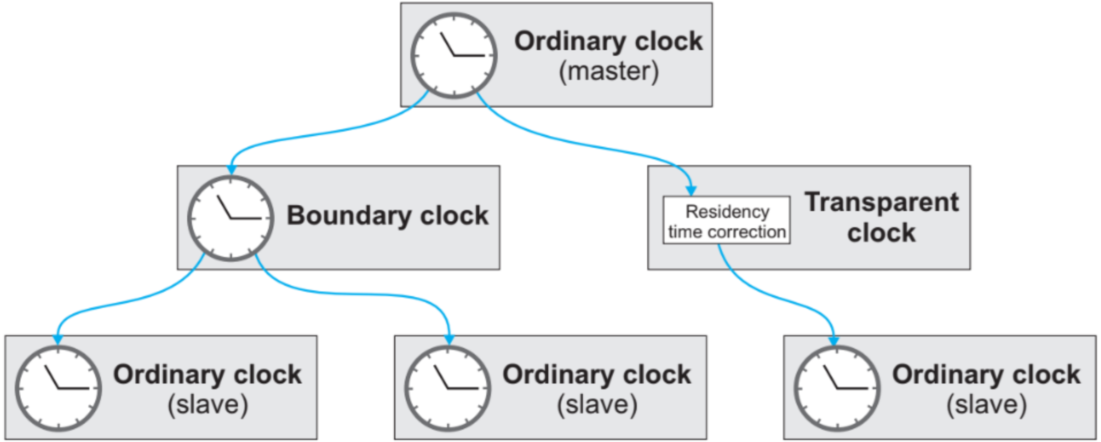


Traditional PTP vs SyncE vs White Rabbit

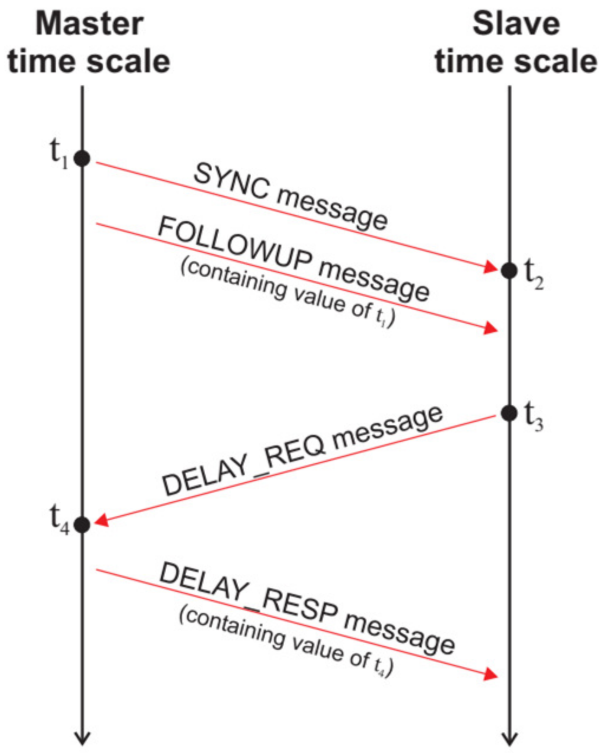
- Traditional PTP
  - All nodes have free-running oscillators
  - Rate of slave clock is adjusted with timestamped packets => high low frequency jitter
  - Timestamping precision is limited to a one clock cycle (typ. 8 ns for Gigabit Ethernet)
  - No method for compensating link asymmetry => likely not relevant in Automotive (?)
- Synchronous Ethernet
  - All network nodes use the same physical layer clock: Clock is encoded in the Ethernet carrier and recovered by the PLL in the PHY
  - PTP is used only for compensating clock offset
  - We can use phase measurements instead of direct timestamping
- PTP-HA (White Rabbit, WR)
  - Monitor phase of bounced-back clock continuously
  - PLL in the slave follows the phase changes measured by the master
  - Performance is equivalent to PTP with messages exchanged every 8 ns

Introduction to PTP

- Ordinary Clocks (OC) are single port devices in master or slave mode
- Boundary Clocks (BC) are multiport devices with a single synchronized local oscillator
- Transparent Clocks (TC) are multiport devices without a local oscillator, but forward packets with adjusted timestamps. Not available for PTP-HA.



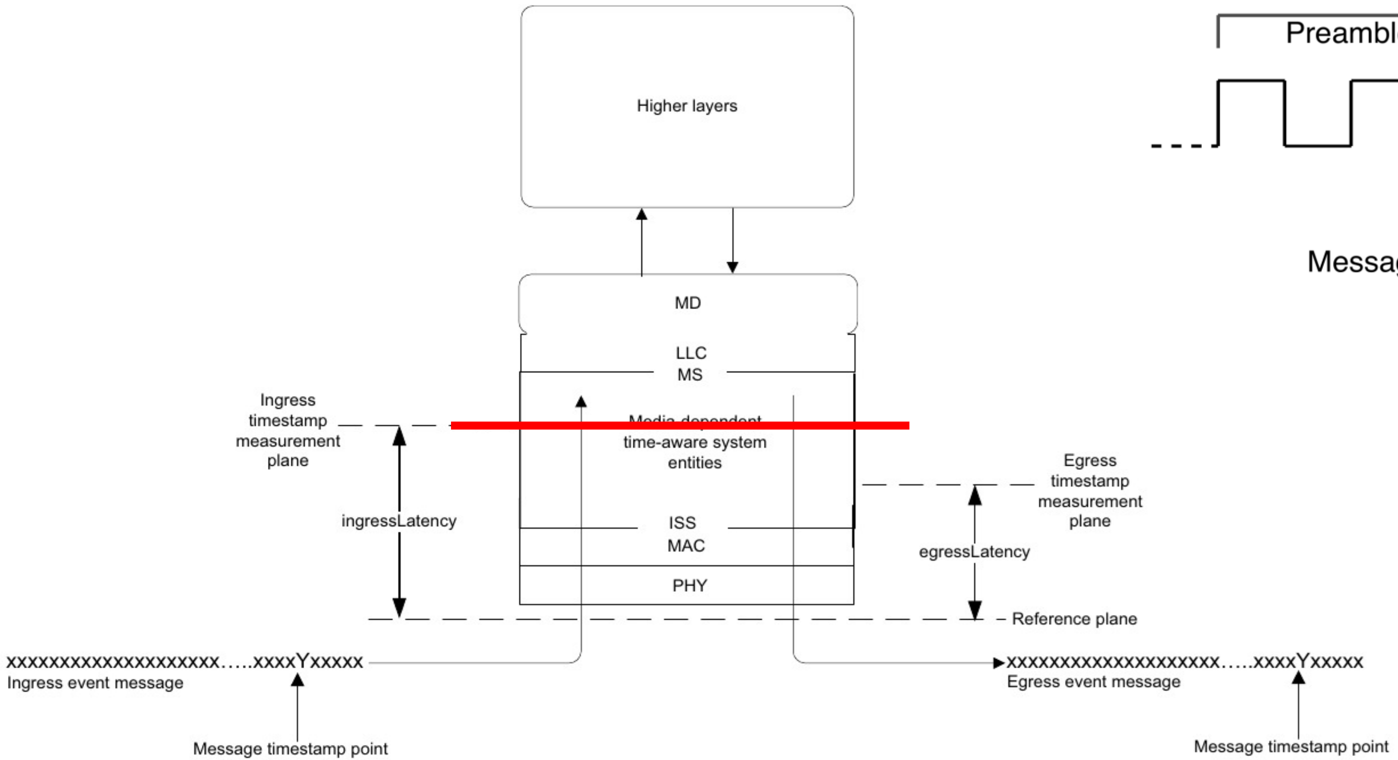
Traditional PTP and PTP-HA Two Step Handshake

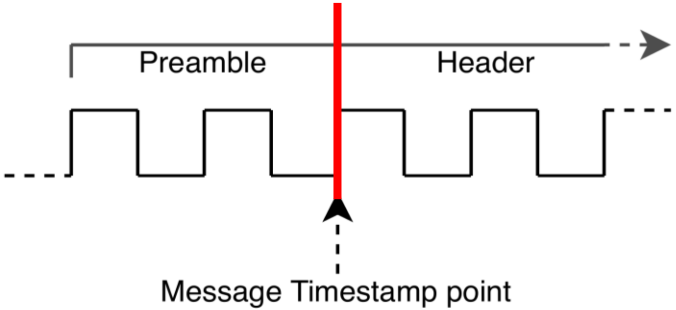


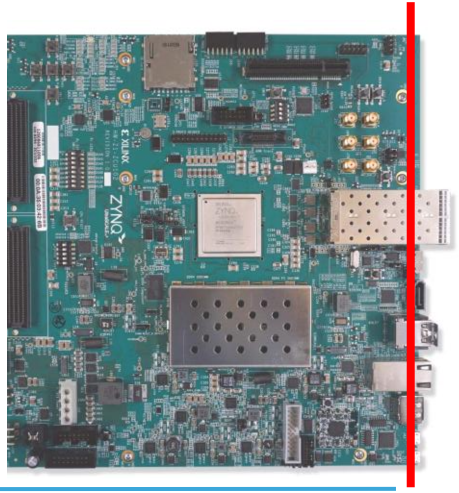
Having values of $t_1 \dots t_4$, slave can:

- calculate one-way link delay:
  $$\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$
- compute clock offset:
  $$offset = t_2 - t_1 + \delta_{ms}$$
- syntonize its clock rate with the master by tracking the value of $t_2 - t_1$

Where does Timestamping happen? The Layers



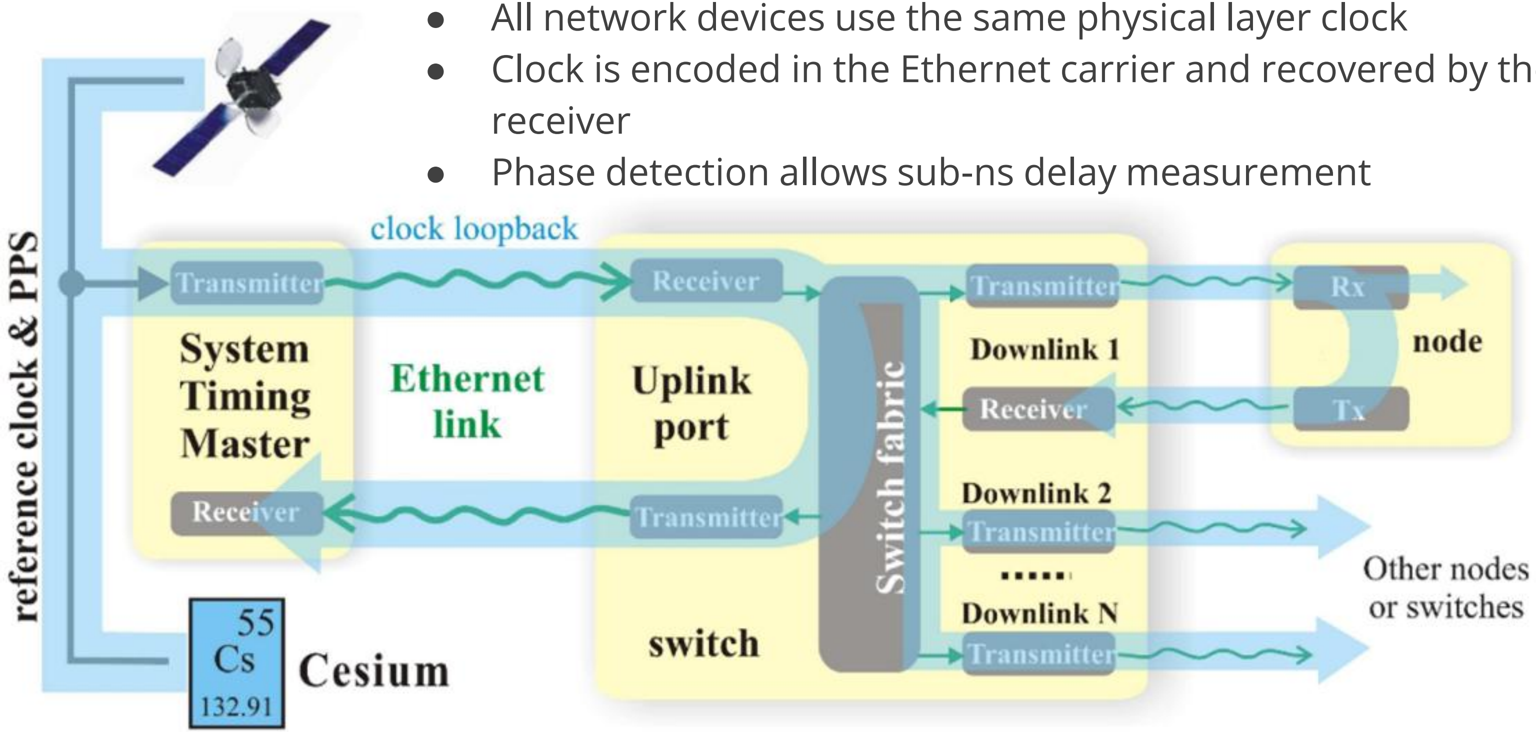




White Rabbit

Layer 1 syntonisation

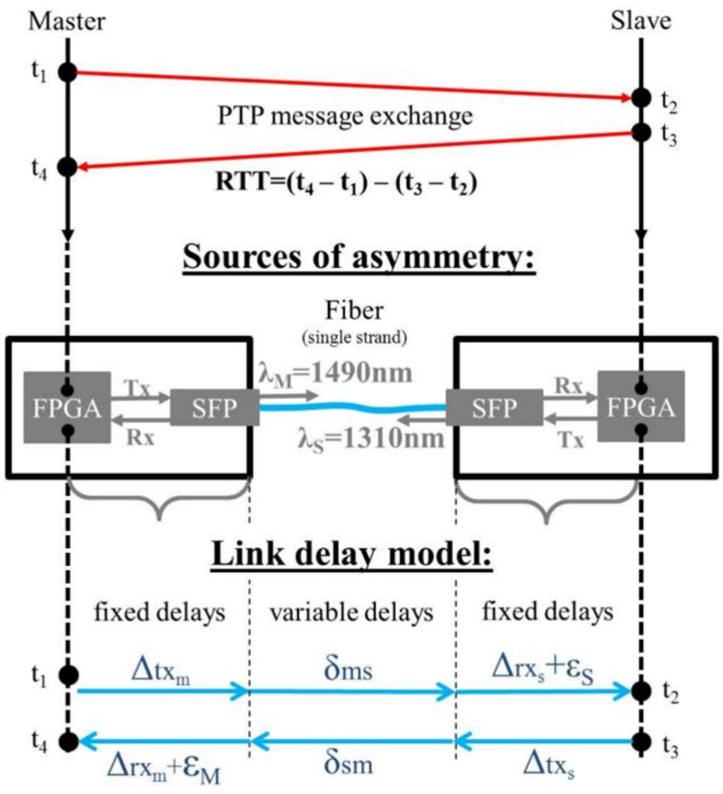
- All network devices use the same physical layer clock
- Clock is encoded in the Ethernet carrier and recovered by the receiver
- Phase detection allows sub-ns delay measurement



White Rabbit

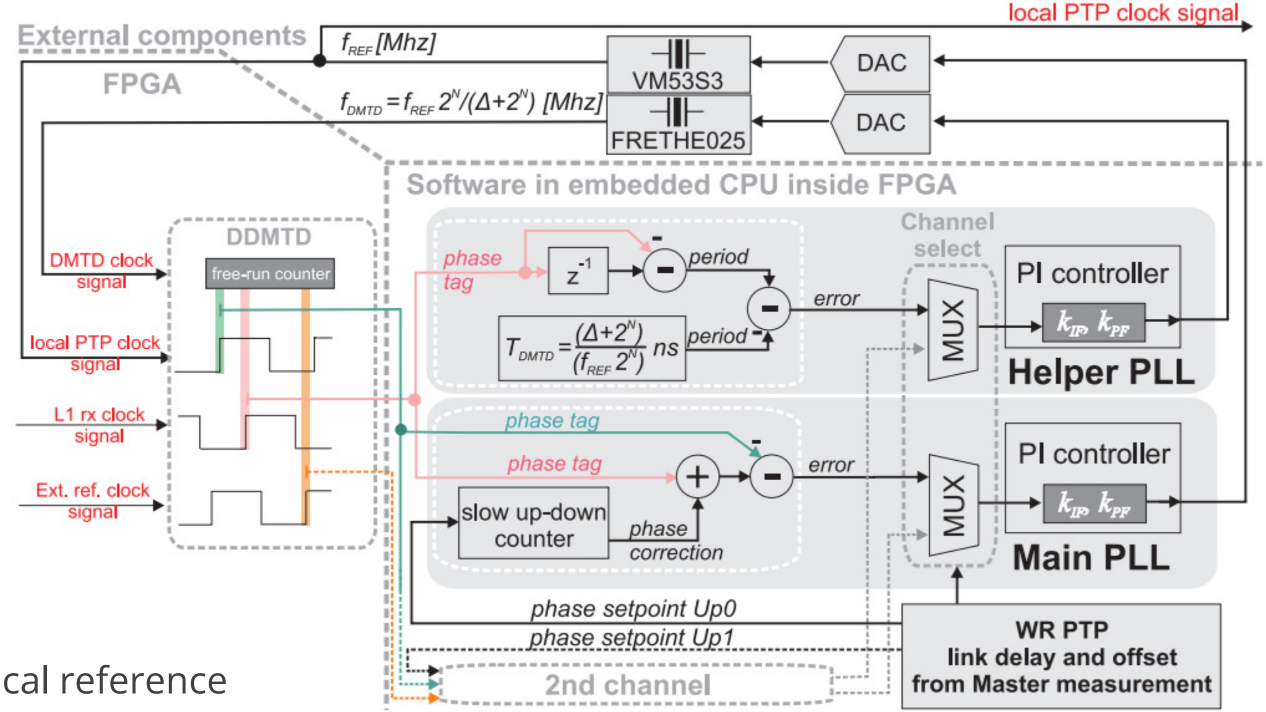
Link Delay Model

- Implements PTP protocol for delay measurement
- Allows for compensation of known fixed delay components (Absolute Calibration)
- Allows for asymmetric link delay modeling
  - Helps to gain the required accuracy
  - Asymmetry sources: FPGA, PCBs, Dispersion (depending on optics), etc.



See: *WR Calibration* [9]

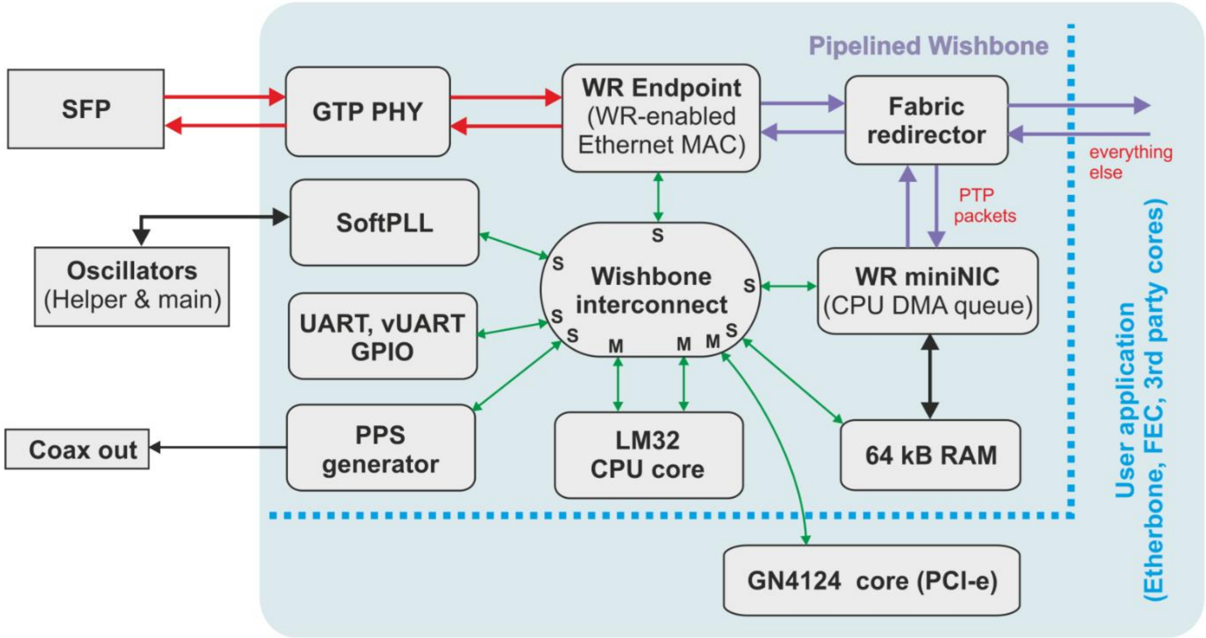
White Rabbit



Clock Control Loop

- A helper clock is the local reference
- Reference (TX) and RX (recovered) clocks are compared to local reference
- Phase is measured overall from one device to another and also compensated for

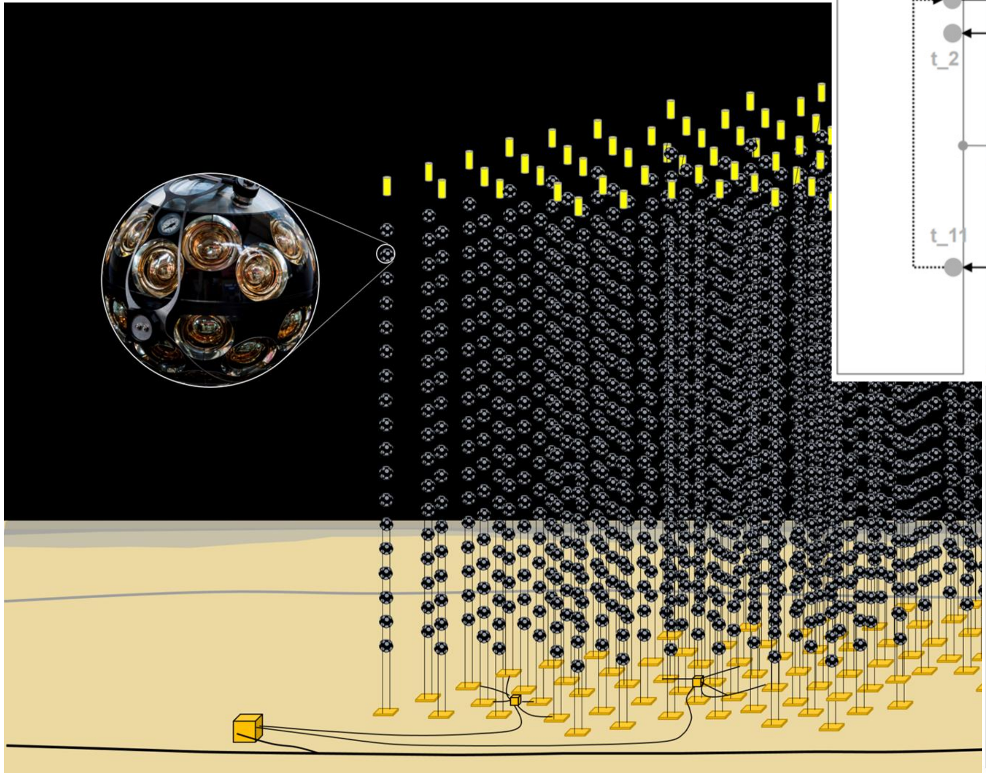
White Rabbit

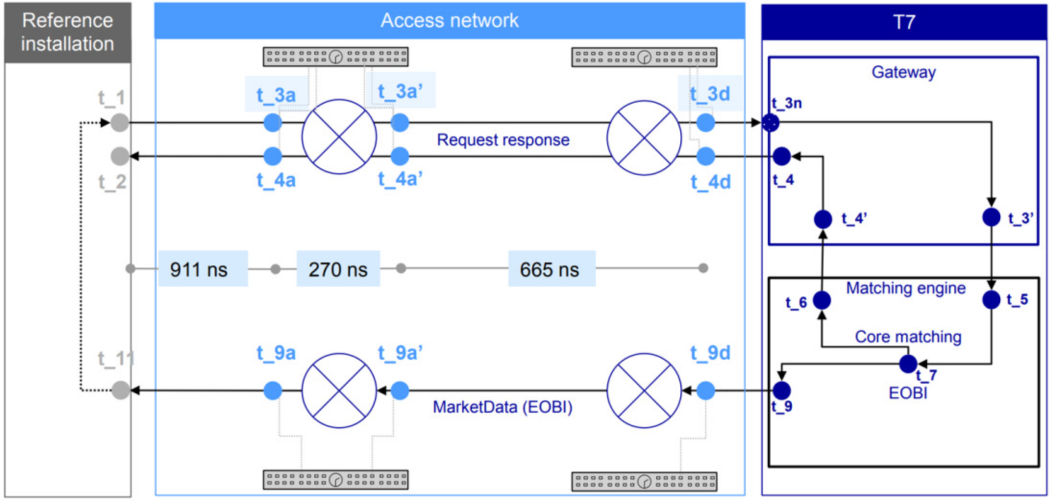


Gateware Block Diagram

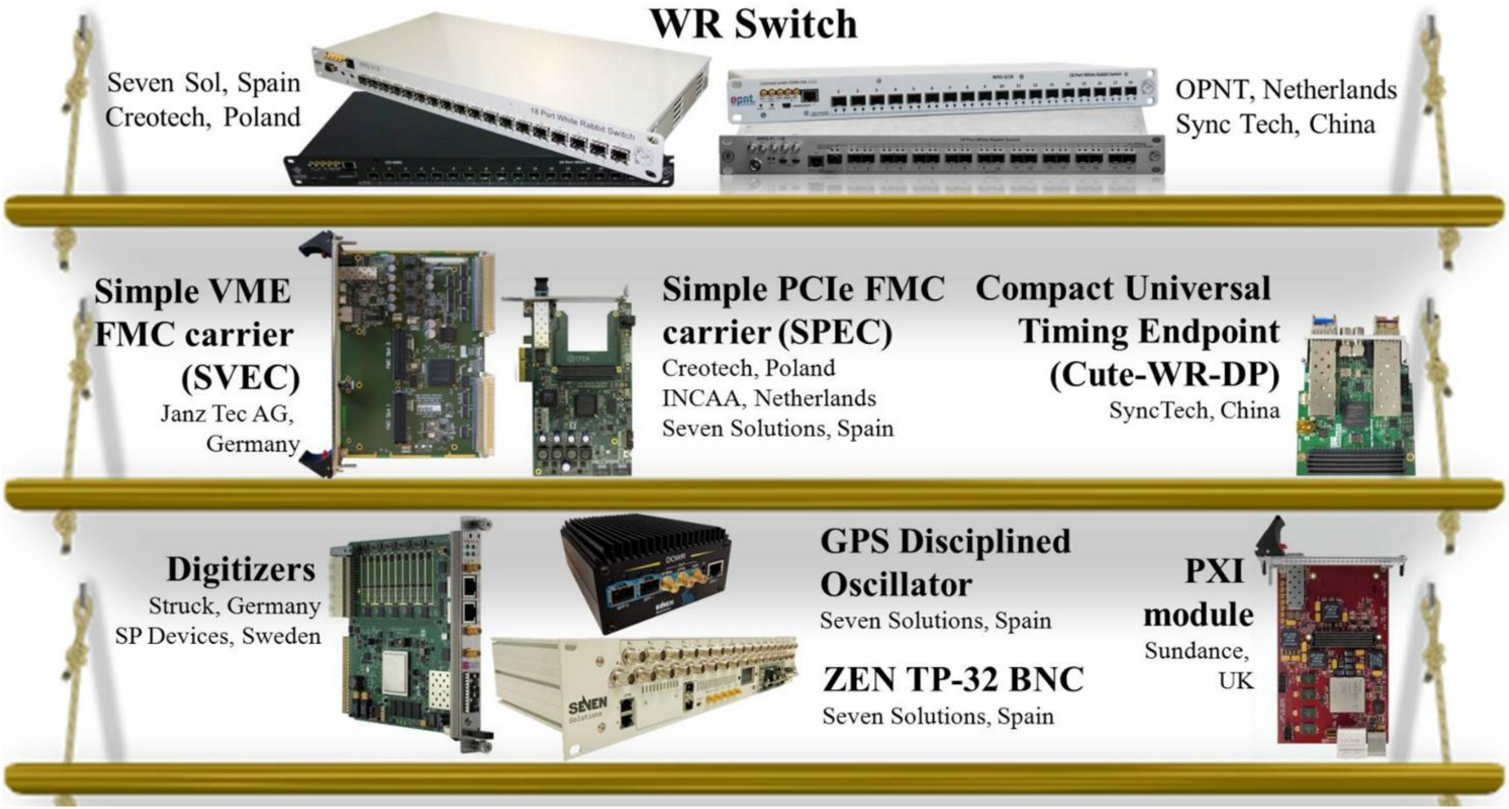
- A RISC-V soft core implements the high-level control loop, CLI and monitoring, GNSS support, etc.
- Peripherals can be used to tag or generate events with with very high precision
- Additional clocks can also be tuned according to the synchronous network clock (AUX clocks)

Original Target Users

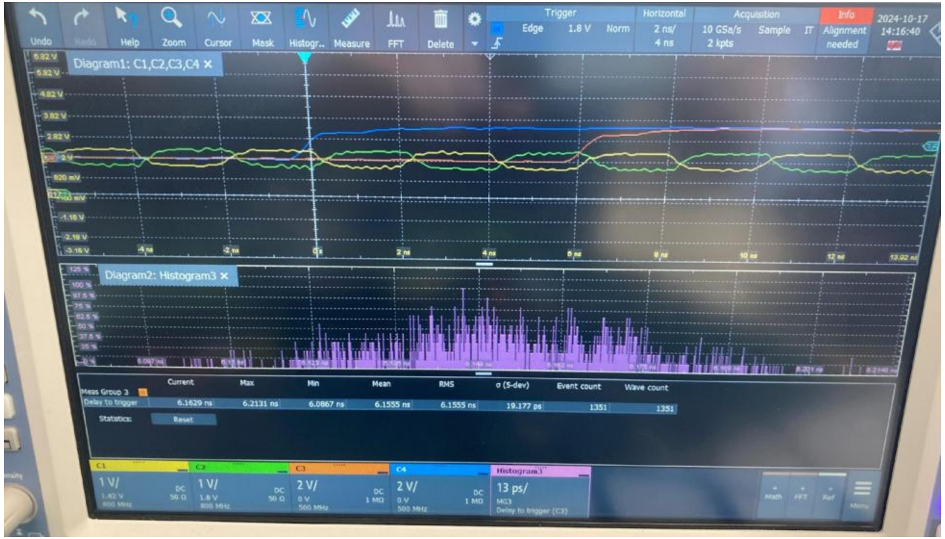


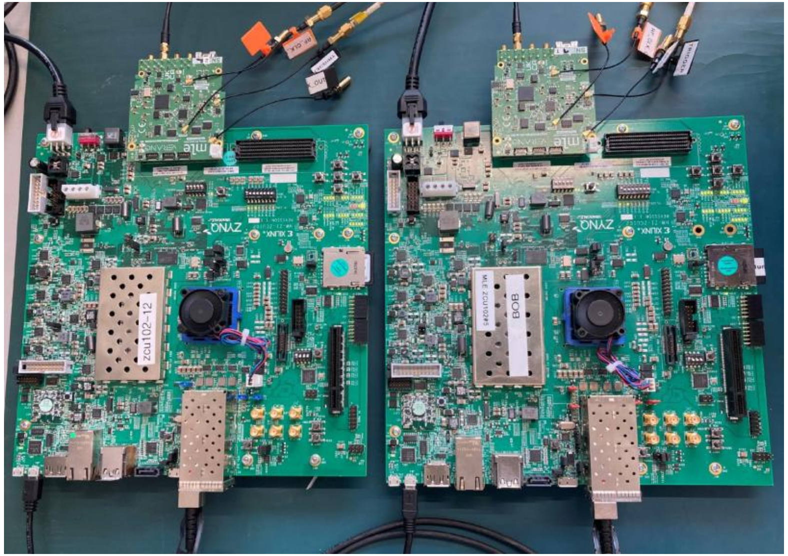


Currently Available Devices (a lot of are OHWR)



White Rabbit on ZCU102





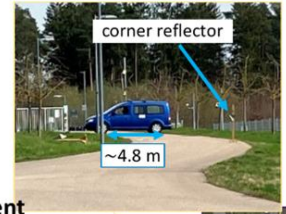
PPS stddev	< 20 ps
PPS Range	< 130 ps
PPS mean	< 6.2 ns
Measurements	1351

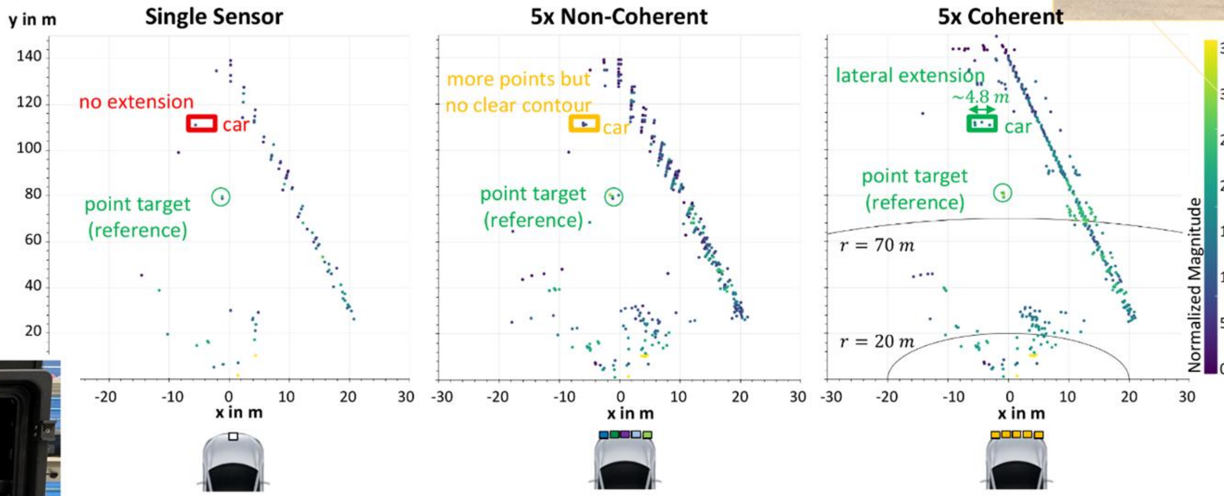
Uncalibrated Device

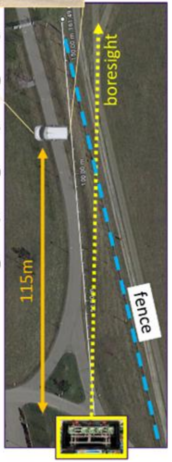
Benefits of coherent RADAR in ADAS

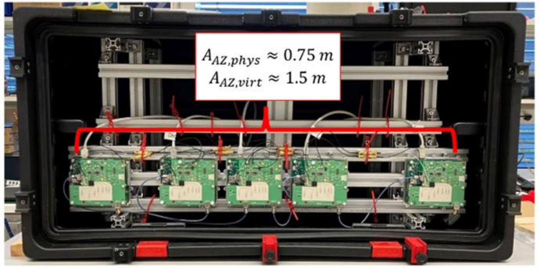
For reference only!
Not sync'ed via WR

Coherent Systems
PoC – Sideways Car



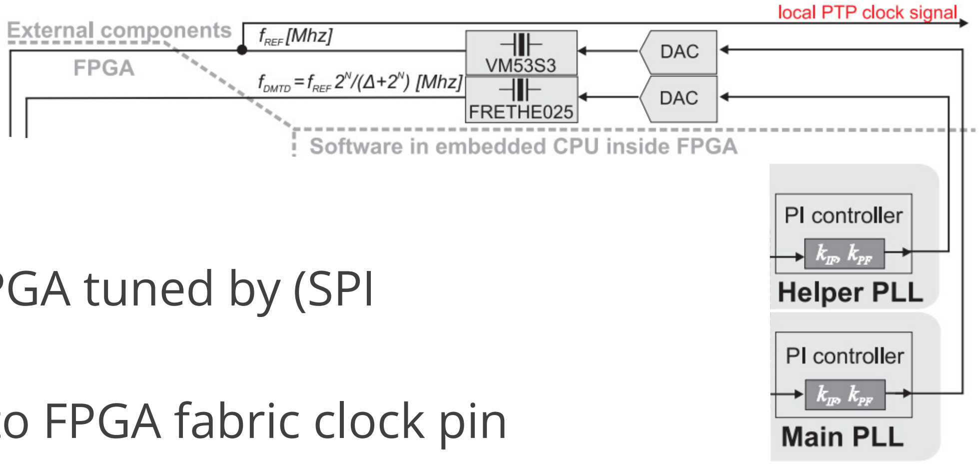






Coherent estimation shows high accuracy (fence reflexes) and lateral extension of car with multiple reflexes.

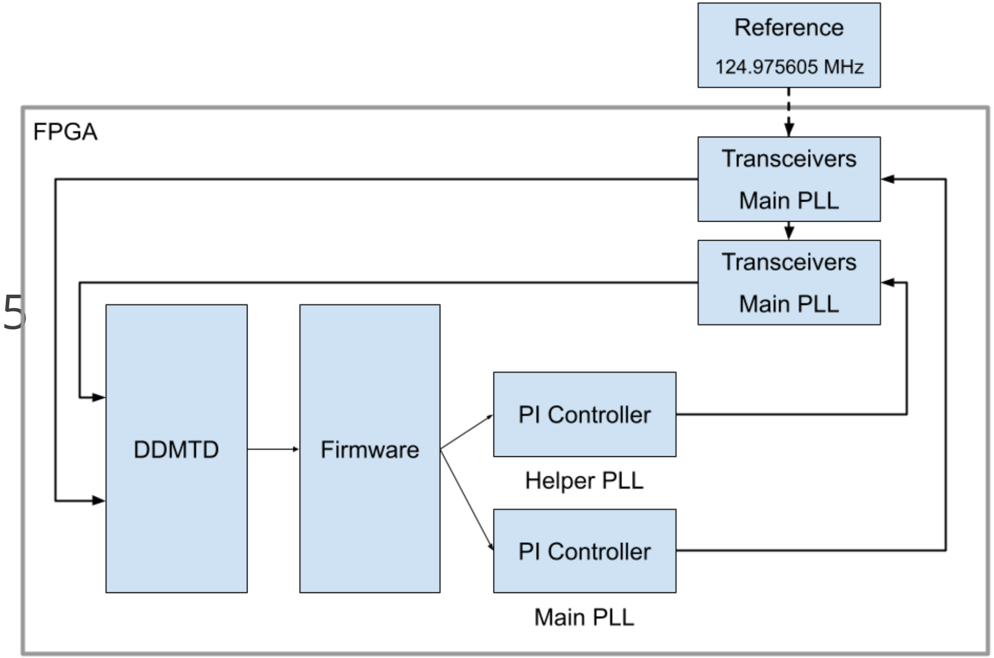
Typical WR Clock Architecture



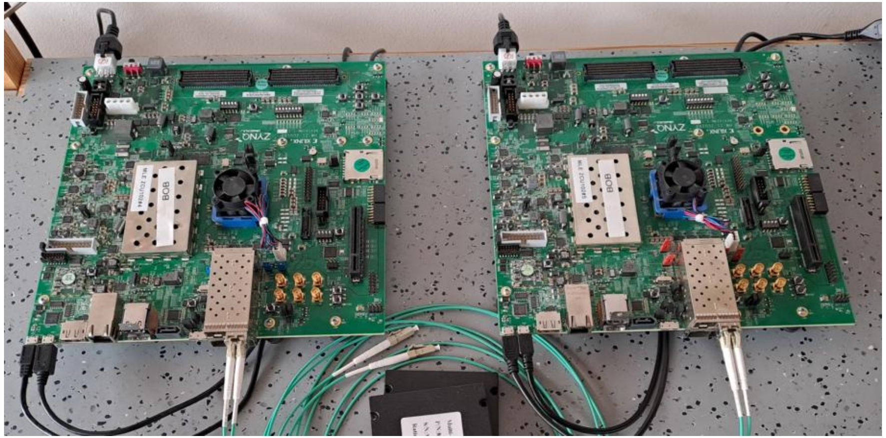
- Two VCOs outside the FPGA tuned by (SPI controlled) DACs
- Helper clock connected to FPGA fabric clock pin
- Main clock (aka transceiver reference clock) connected to FPGA fabric clock pin and transceiver reference clock pin via clock fanout buffer

Light Rabbit Clock Architecture (FPGA only)

- Leveraging AMD ZCU102 MPSoC GTH Transceiver QPLLs
- Requires multiple GTH Quads
- Requires external fixed GTH reference clock slightly below 125 MHz
- Frequency is adjusted using the QPLL “SDM” feature



Light Rabbit on AMD ZCU102



Uncalibrated Device

PPS stddev	< 24 ps
PPS Range	< 170 ps
PPS mean	< 1.4 ns
Measurements	7304

Overview and Results

1 GbE	gPTP	PTPv2 HA (LR)	PTPv2 HA (WR)
Communication	Asynchronous	Synchronous	Synchronous
Precision	< 110 ns	< 170 ps	< 130 ps
Calibration	N/A	Partially Achieved	Done

Let’s collaborate and further explore the opportunities, raise the TRL and solve open problems!

Some of the Problems:
Timing loops, Transition between masters, System Integration via PCIe PTM, …