Image Signal Processing for a Camera Monitor System with an ZYNQ FPGA

M. Sc. Steffen Jannik Maier
Hochschule Ulm
26.06.2018

Programmable Processing for the Future and Autonomous Car
– From classical FPGA to heterogeneous MPSoC
Motivation

Image Signal Processing for a Camera Monitor System with a ZYNQ FPGA

› Better aerodynamics
› Reduction of blind spot
› Data processing possible
  o Object tracking
  o Blind spot detection
› ...

Concept car of the Daimler AG [Media.Daimler.com]
Table of contents

› Introduction of the topic

› Definition of the components
  o Camera
  o Monitor
  o Normative Framework based on ISO 16505 and UN Regulation No. 46
  o The image Signal Processing device

› Description of the Signal Processing functions
  o Data Processing concept
  o Image Signal Processing system
  o Data Preprocessing
  o Information visualization
  o Resource management

› Conclusion
Introduction of the topic

Automated Driving

Five Levels of Vehicle Autonomy

Level 0: No automation. The driver is in complete control of the vehicle all the time.

Level 1: Driver assistance. The vehicle can assist the driver or take control of either the vehicle's speed, through cruise control, or its lane position, through lane guidance.

Level 2: Occasional self-driving. The vehicle can take control of both the vehicle's speed and lane position in some situations, or example on limited-access freeways.

Level 3: Limited self-driving. The vehicle is in full control in some situations, monitors the road and traffic, and will inform the driver when it or she must take control.

Level 4: Full self-driving under certain conditions. The vehicle is in full control for the entire trip in these conditions, such as urban ride-sharing.

Level 5: Full self-driving under all conditions. The vehicle can operate without a human driver or occupants.

Source: SAE & NHTSA

SAE Levels [Forbes.com]

Goal: Embedded flexible platform to develop and investigate signal processing toolchains and architectures

RC-Car [HSU]
Introduction of the topic

Camera Monitor System (CMS)

Definition of a Camera Monitor system by [HSU & 1]
Definition of the components

The Camera

› Avnet FMC-Module
  - HDMI input and output
  - LCED-Interface for camera connection
  - Parallel FMC-Interface for ZYNQ-Board connection

› ON Semiconductor VITA-200 Image Sensor
  - Resolution 1920 x 1080 Pixel
  - Max. 92 fps
  - LCED-Interface (LCD Coaxial Embedded Display Interface) for data transmission
  - LVDS and SPI-Interface for configuration

› LCED-Interface
  - Developed by TE [TE.com]
  - 2.7 Gbps/lane data rate
  - 10.8 Gbps bandwidth
  - Four lanes
Definition of the components

The Monitor

› The used Monitor is standard 24 Inch PC component
  o Minimum 1024 x 768 Pixels
  o Minimum 60 fps
  o HDMI-Interface connection

› Vehicle Monitor for Class III mirrors
  o 8 Inch Monitor
  o 800 x 480 Pixel
  o 200 Mbit/s data rate
  o Minimum 30 fps

› Monitor has to be ISO 16505 and UN Reg. No. 46 confirm according to [2 & 3]

Laboratory Monitor with test image [HSU]
Definition of the components


› Standard and regulation covering min. requirements and test methods for CMS
› Field of view shall cover at least the field of view of the conventional mirror (horizontal & vertical)
› Resolution defines minimum distinguishable details
› Location of the Monitor inside of vehicle is defined
› Image quality is defined for
  o Artefacts / Smear
  o Blooming and lens flare
  o Color noise
  o Sharpness
  o Pixel faults
  o Etc.
› Timing behavior also set, minimum frame rate of 30 Hz (15 Hz at low light condition)
› Overlays
Definition of the components

The image Signal Processing device

› ZYNQ-7000 SoC Evaluation Board (ZC702)
› XC7Z020 chip
› Definition of the pictured components
  1. Camera
  2. Interface: LCEDI
  3. FMC IMAGEON HDMI Module
  4. HDMI/DVI Output
  5. JTAG USB Port
  6. UART USB Port
  7. DC current connector

Hardware setup of the mirror replacement system [HSU]
Definition of the components

The Xilinx ZYNQ ZC702 chip
- Part of the ZYNQ-7000 all programmable SoC family
- Includes a Dual-Core ARM Cortex-A9 Processor and an FPGA
  - The FPGA:
    - 85 K Logic Cells
    - 4.9 Mb Block RAM
    - 220 DSP Slices
    - 200 I/O Pins
    - 200 MHz Clock
  - The ARM Cortex-A9:
    - Dual-Core
    - Up to 2 GHz Clock
    - 8 MB Cache
Description of the Signal Processing functions

Data Processing concept

› One base of image signal processing is object recognition
› Input to system is an image
› Image consists of pixel
› Each pixel carries little information
› Large number of pixels describe scene
› Preprocessing already implemented
› Parameters configurable
› System architecture can be adjusted to different use cases

Image Processing pyramid defined by [4]
Description of the Signal Processing functions

Image Signal Processing system

Data preprocessing
- Raw data

Data processing
- Data

Information visualization
- Information

Image

Image Signal Processing toolchain design by [HSU]
Description of the Signal Processing functions

Implemented image Signal Processing system on the FPGA [HSU & 5]
Data preprocessing is used to reduce size of image

<table>
<thead>
<tr>
<th>Processing Block</th>
<th>Description</th>
<th>Image Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw data input</td>
<td>Raw data of camera in RGB format</td>
<td>1920 x 1080 Pixel, 24 Bit Pixel depth</td>
</tr>
<tr>
<td>Color space converter</td>
<td>Transformation RGB to YCbCr</td>
<td>1920 x 1080 Pixel, 24 Bit Pixel depth</td>
</tr>
<tr>
<td>Chroma resampler</td>
<td>Reduces color saturation (4:4:4 -&gt; 4:2:2)</td>
<td>1920 x 1080 Pixel, 16 Bit Pixel depth</td>
</tr>
<tr>
<td>ROI-generator</td>
<td>Cuts out Region Of Interest</td>
<td>1024 x 768 Pixel, 16 Bit Pixel depth</td>
</tr>
</tbody>
</table>

Data preprocessing table [HSU & 6]

Data reduction:
- Raw Data: 5.93 MB per image
- After compression: 1.50 MB per image
- Factor 3.95 smaller
- Data Processing is much faster
## Description of the Signal Processing functions

### Information visualization - overlays

<table>
<thead>
<tr>
<th>ISO 16505</th>
<th>UN Regulation No.46</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Visualization</strong></td>
<td>Only transparent overlays allowed</td>
</tr>
<tr>
<td></td>
<td>Any overlays (regardless of their transparency) are considered as an obstruction</td>
</tr>
<tr>
<td><strong>Duration</strong></td>
<td>Only temporary</td>
</tr>
<tr>
<td></td>
<td>Only temporary</td>
</tr>
<tr>
<td><strong>Information</strong></td>
<td>Only driving related visual information</td>
</tr>
<tr>
<td></td>
<td>Only rearward driving related visual information</td>
</tr>
<tr>
<td><strong>Size</strong></td>
<td>Size unlimited</td>
</tr>
<tr>
<td></td>
<td>Maximal size of each overlay is 2.5% of the area which displays the minimum required field of vision. Overlays have to be included when calculating the obstructions within the required field of view (obstructions are limited to a maximum of 15% for Class I mirrors and to a maximum of 10% for all other classes)</td>
</tr>
</tbody>
</table>

**Comparison of the requirements for overlays of ISO and UN Regulation [1]**
Description of the Signal Processing functions

Information visualization

Class II

Object detection and tracking examples [1]

Class I
Description of the Signal Processing functions

Information visualization

› Each Overlay defines a new Layer
› Layer 0 is the original image
  o Bypass image for minimum delay
› All other Layers are processing solutions
  o Transparency defined
  o Color configurable

Picture of an example image for the output generated by the test plot generator (TPG) [HSU]
Description of the Signal Processing functions

ZYNQ FPGA Resource summary

› Currently implemented design uses:
  - 7000 Flip Flops (7%)
  - 6300 LUTs (12%)
  - 181 Memory elements (1%)
  - 10 DSPs (5%)

› The power consumption is about 2W (according to Xilinx Power estimator)

› The current frame rate is 30 fps

*Implemented on Chip design, left the used resources, right routing [HSU]*
Conclusion

› HSU designs a development platform enabling investigation of signal processing and architectures
› Embedded flexible platform based on Xilinx ZYNQ 7000 SoC used for a CMS research
› System design using Vivado, VHDL and IP Cores
› System parameter based on the normative framework of ISO 16505:2015 and UN Regulation No. 46
› Process separated into three parts
  o Data preprocessing
  o Data processing
  o Information visualization
› First preprocessing operations for low level tasks are already implemented
Bibliography

1. „Handbook of Camera Monitor Systems“, Anestis Terzis eds., Springer International Publishing AG, Switzerland 2016


3. „Addendum 45: Regulation No. 46“, United Nations, 2013

4. „Design for Embedded Image Processing on FPGAs“, Donald G. Bailey, John Wiley & Sons, Singapore 2011

5. „Schaltungs-Entwurf für ein Fahrerassistenzsystem“, H.-M. Bühler, A. Maier, Studienarbeit, HS Ulm, 2014

6. „Entwurf einer Bildverarbeitungs-Schaltung auf Basis eines SoC-FPGA“, M. Schmied, J. Schneider, Studienarbeit, HS Ulm, 2015

7. „Entwurf und Bewertung eines Kamera-Monitor-Systems als Fahrzeugspiegelersatz nach ISO 16505“, M. Merlini, Bachelorarbeit, HS Ulm, 2015
Image Signal Processing for a Camera Monitor System with an ZYNQ FPGA

Thank you for your attention!

M. Sc. Steffen Jannik Maier
Hochschule Ulm,
Eberhard-Finckh-Str. 11, 89075 Ulm
Jannik.maier@hs-ulm.de
+49 (0731) 50-16865